# LOW POWER RECONFIGURABLE MICROWAVE CIRCUITS USING RF MEMS SWITCHES FOR WIRELESS SYSTEMS

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# LOW POWER RECONFIGURABLE MICROWAVE CIRCUITS USING RF MEMS SWITCHES FOR WIRELESS SYSTEMS

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*To my parents*

谨以此书献给我的父母

郑崇海
郭爱霞

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# SUMMARY

This dissertation presents the research on several different projects. The first project is a via-less CPW RF probe pad to microstrip transition; The second, the third, and the fourth one are reconfigurable microwave circuits using RF MEMS switches: an X-band reconfigurable bandstop filter for wireless RF frontends , an X-band reconfigurable impedance tuner for a class-E high efficiency power amplifier using RF MEMS switches, and a reconfigurable self-similar antenna using RF MEMS switches. The first project was developed in order to facilitate the on-wafer measurement for the second and the third project, since both of them are microstrip transmission line based microwave circuits. To measure the s-parameters of microwave circuits, a CPW footprint is needed, thus, a transition from a CPW RF probe pad to a microstrip transmission line is required. A thorough study of the via-less CPW RF probe pad to microstrip transition on silicon substrates was performed and general design rules are derived to provide design guidelines. This research work is then expanded to W-band via-less transition up to 110 GHz. The second project is to develop a low power reconfigurable monolithic bandstop filter operating at 8, 10, 13, and 15 GHz with cantilever beam capacitive MEMS switches. The filter contains microstrip lines and radial stubs that provide different reactances at different frequencies. By electrically actuating different MEMS switches, the different reactances from different radial stubs connecting to these switches will be selected, thus, the filter will resonate at different frequencies. The third project is to develop a monolithic reconfigurable impedance tuner at 10 GHz with the cantilever ohmic (DC) contact MEMS switch. The impedance tuner is a two port network based on a "3bit-3bit" digital design, and uses 6 radial shunt stubs that can be selected via integrated DC contact MEMS switches. By selecting different states of the switches, there will be a total of $2^6 = 64$ states, which means 64 different impedances will be generated at the output port of the tuner. This will provide a sufficient tuning range for the output port of the power amplifier to maximize the power efficiency. The last project is

to integrate the DC contact RF MEMS switches with self-similar planar antennas, to provide a reconfigurable antenna system that radiates with similar patterns over a wide range of frequencies. Different issues encountered during the integration of the MEMS switches and the DC bias lines with the single antenna was addressed. The final model radiates at three widely separated frequencies with very similar radiation patterns. The proposed concept can be extended to reconfigurable linear antenna arrays or to more complex antenna structures with large improvements in antenna performance.

# CHAPTER I

# INTRODUCTION

This dissertation presents the research work on the microstrip transmission line based reconfigurable microwave circuits using RF MEMS (radio frequency micro-electro-mechanical system) switches. In order to facilitate the on-wafer measurements, another thrust of this research work was also conducted to derive the design guidelines for a via-less CPW (coplanar waveguide) RF probe pad to microstrip transition up to 110 GHz. The via-less feature is emphasized here since it will dramatically simplify the fabrication process of integrated microwave circuits, thus, reduce their cost. The design rules obtained have been intensively used by the researchers inside and outside our research group. This work is presented in Chapter 2.

To realize the reconfigurability, RF MEMS switches were used. RF MEMS switches' electro-mechanical performance has been studied and analyzed; MEMS switches were designed, fabricated, and tested using an Agilent 8510C vector network analyzer. The measured results were curve fitted to the simulated results from the equivalent circuit model, to extract the off-state capacitance and the on-state capacitance and resistance. In this dissertation, two types of RF MEMS switches are utilized: one is the cantilever capacitive RF MEMS switch; the other is the cantilever DC contact RF MEMS switch. This work is presented in Chapter 3.

Chapters 4 to 6 present the reconfigurable microwave circuits using RF MEMS switches and the via-less transitions developed previously.

Chapter 4 introduces an X-band reconfigurable bandstop filter using RF MEMS switches for wireless RF frontend. This is a low power reconfigurable monolithic bandstop filter operating at 8, 10, 13, and 15 GHz, using cantilever beam capacitive RF MEMS switches. The filter contains microstrip transmission lines and radial stubs that provide different reactance

at different frequencies. By electrically actuating different MEMS switches, different reactances from different radial stubs connecting to these switches will be selected; thus the filter will resonate at different frequencies.

Chapter 5 presents an X-band reconfigurable impedance tuner for a class-E high efficiency power amplifier using RF MEMS switches. This is a monolithic reconfigurable impedance tuner at 10 GHz using cantilever beam DC contact RF MEMS switches. The tuner is a two port network based on a "3bit - 3bit" digital design, and uses 6 radial shunt stubs that can be selected via the integrated DC contact MEMS switches. By selecting different states of the switches, there will be a total of $2^6 = 64$ states, which means 64 different impedances can be generated at the output port of the impedance tuner. This will provide a sufficient tuning range for the output of the class-E power amplifier, to achieve optimum output power efficiency. The output impedance range was provided by the University of Colorado.

Chapter 6 entails a self-similar silicon based reconfigurable fractal antenna using cantilever beam DC contact RF MEMS switches. Since it acts as a dipole antenna, a different transition (CPS to CPW transition) was needed to facilitate the on-wafer probing. The fractal antenna design was done at the University of New Mexico, while the circuits' layout generation, process flow development, fabrication, and measurements were done at the Georgia Institute of Technology. The testing was done using an Agilent 8510C vector network analyzer.

## *1.1 Origin and History of the Problem*

RF MEMS switch technology has been introduced during the last 10-15 years as a viable alternative with superior RF performance over traditional semiconductor switches, such as pin diodes and FET transistors. It has also paved the way for the development of revolutionary RF circuits that can be potentially used in the next generation of broadband, wireless, and intelligent communication and radar systems. Many researchers have been focusing recently on the development of miniaturized, low power and low cost RF/microwave circuits with RF MEMS switches [1–5]. For this reason, several different types of MEMS

switches have been developed both at academic institutions and in industry. They can be classified as follows: 1) capacitive [3], [6] or DC contact [4], [5] MEMS switches; 2) air bridge [3] or cantilever beam [4,5] MEMS switches. The RF/microwave and the mechanical behavior of these MEMS switches have also been characterized [7–10]. Because of their superior RF performance (low loss, low power and low intermodulation distortion), RF MEMS switches have been used in a variety of RF circuit applications: tunable microwave filters [11–14], tunable phase shifters [15], tunable antennas [16] and tunable matching networks [17].

The development of two different types of microstrip transmission line based reconfigurable microwave circuits using RF MEMS switches is involved in this dissertation: the first one is a reconfigurable bandstop filter, and the second one is a reconfigurable impedance tuner. The useful application of the first project is to suppress the spurious and image frequencies when the microwave receiver experiences interferences. The reconfigurable impedance tuner is used to provide a sufficient output tuning range for an X-band class-E power amplifier. Since both projects are microstrip transmission line based, a transition between the microstrip line to the CPW RF probe pad is needed to facilitate the on-wafer measurement. The last presented reconfigurable microwave circuit is a reconfigurable fractal antenna, which is mainly focused on integrating the RF MEMS switches and DC bias lines to the antenna; the reconfigurable antenna fabrication, and measurements.

Microstrip transmission lines are used in the reconfigurable microwave circuits' design because of its compact size, ease of fabrication, and low cost. However, the low cost and rapid characterization of microwave integrated circuits currently requires coplanar waveguide probe pads. To achieve the highest possible integration, while maintaining each circuit's effective performance, transitions are needed to reduce the mismatch and coupling between different circuit elements. To simplify the fabrication process and lower the fabrication cost, a via-less transition is very much needed. In order to find out the general design rules for this via-less transition and provide design guidelines, the project "via-less CPW RF probe pad to microstrip transition" was defined.

A reconfigurable bandstop filter is one type of very important tunable filters in RF

receivers for wireless communication and radar systems. This dissertation presents a monolithic, reconfigurable, microstrip-based bandstop filter using cantilever beam capacitive RF MEMS switches. Many studies have been done on the reconfigurable filter design, but most of them are bandpass or lowpass filters at different frequency bands with tunable elements, such as MEMS switches or varactors. No reconfigurable bandstop filter has been found to be reported so far. The goal of this work is to develop a four-state or "2-bit" tunable bandstop filter from 8-15 GHz. More specifically, the filter is designed to have a notch at 8, 10, 13, and 15 GHz, respectively, whereby each notch can be selected electronically by activating the appropriate MEMS switches. One useful application of this filter is to provide a good image frequency rejection for RF/microwave front-end transceivers. The cantilever beam capacitive MEMS switch with electrostatic actuation was chosen for the filter design since it is easier to design and fabricate.

The second type of microwave circuit presented in this dissertation is a reconfigurable impedance tuner using cantilever beam DC contact RF MEMS switches. To the author's best knowledge, this is the first monolithic, microstrip based reconfigurable tuner on a silicon substrate using DC contact MEMS switches for maximizing the efficiency of X-band power amplifiers. Few studies have been done in the area of reconfigurable tuner design so far: A hybrid tuner with capacitive RF MEMS switches has been reported in [17] that matches impedances equivalent to three quadrants of the Smith chart with a max VSWR of 99 at 20 GHz. That tuner exhibited variations between the simulated and measured results, as well as relatively large size due to its hybrid nature. The development of such hybrid tuners for the matching of the output or input impedance of an RF power amplifier can be quite challenging. Other impedance tuners that have been reported utilize resonant unit cells and variable stub-lengths realized by micromachined capacitors and MEMS switches [18]. This tuner achieved a tuning range equivalent to two quadrants of the Smith chart and a maximum VSWR of 32.3 at Ka-band. More recently, a 4 and 8 element impedance tuners with MEMS switches for noise measurements and load-pull measurements from 10 to 28 GHz have been developed [19].

The application for the tuner presented in this dissertation is efficiency optimization of

X-band class-E power amplifiers [20]. In the class-E switched mode of operation, the active device is driven hard into saturation, and small device-to-device and parasitic variations have a great effect on the efficiency. A load-pull technique combined with the measurements of 30 hybrid class-E 10 GHz PAs determines the optimal output impedance range required for the output tuner.

Last, for the reconfigurable antennas, the cantilever DC contact RF-MEMS switches were integrated with self-similar planar antennas to provide a reconfigurable antenna system that radiates with similar patterns over a wide range of frequencies [21]. The single fractal antenna was designed at the University of New Mexico. My contributions are as follows: providing the circuit model for the DC contact RF MEMS switches; integrating RF MEMS switches with the antenna; implementing the design procedure for the DC bias lines and integrating them with the rest of the circuitry; generating the circuits' layout for fabrication; developing the fabrication process flow; and testing the antenna s-parameters with a vector network analyzer. The radiation pattern was measured at NASA Glenn Research Center. The measured results were compared with the simulations, the data was analyzed, and future improvements for integrated antenna design were proposed.

## *1.2 Via-Less CPW RF Probe Pad to Microstrip Transition Background*

The via-less CPW RF probe pad to microstrip transitions were developed to facilitate the on-wafer measurements for microstrip transmission line based microwave circuits. In order to measure the s-parameters of RF/microwave circuits, a CPW footprint is needed; thus, a transition from a CPW RF probe pad to a microstrip transmission line is required. Based on this need, the research work was conducted. A thorough study of the via-less CPW RF probe pad to microstrip transition on silicon substrate was performed and general design rules were derived to provide the design guidelines.

The transitions were designed and fabricated on a silicon substrate with a center frequency of 20 GHz. The Method of Moments (MoM) was used to both verify the experimental results and optimize the design. The top view of the via-less transition is shown in

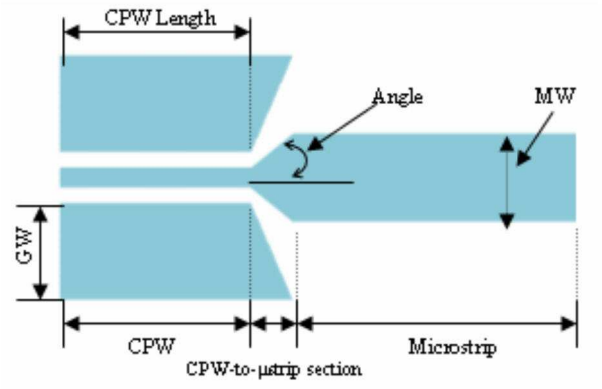



**Figure 1:** Top view of the CPW to microstrip transition structure requiring no vias (bottom ground plane everywhere)

Figure 1.

Figure 1 shows the schematic of the CPW to microstrip transition. The complete structure consists of a CPW section, a CPW-to-microstrip transition section, and a microstrip section. In the intermediate transition section, the width of the CPW signal strip is gradually increased to match the width of the microstrip transmission line. At the same time, the gap between the ground planes and the signal line is widened to retain a 50 Ω characteristic impedance, in order to match that of the microstrip line, and minimize the reflections. As shown in Figure 1, 'GW' is the width of the CPW ground plane width, 'MW' is the width of the microstrip line, which is 360 $\mu$m to obtain a 50 Ω characteristic impedance. The substrate is a high resistivity silicon wafer with $\epsilon_r = 11.7$, $\rho > 8000$ Ω-cm, a thickness of 400 $\mu$m, and a 1 $\mu$m thick $SiO_2$ layer on the silicon wafer that acts as the insulation layer. Where, $\epsilon_r$ is the relative dielectric constant, and $\rho$ is the resistivity of the silicon wafer. The signal line width of the CPW is 104 $\mu$m, while the slot (gap) width is 80 $\mu$m. In order to better understand this transition and derive the design rules, the CPW section length ('CPW Length' in Figure 1) and the angle ('Angle' in Figure 1) of the transition between the CPW and microstrip line were studied and varied. The length of the intermediate section can be calculated as long as the angle is given.

This work was then extended to the W-band, which shows excellent performance. Figure 2 shows that the measured and simulated insertion loss agree very well from 20 GHz to 100 GHz, with an average loss about 0.4 dB; while from 50 GHz to 80 GHz, the insertion loss

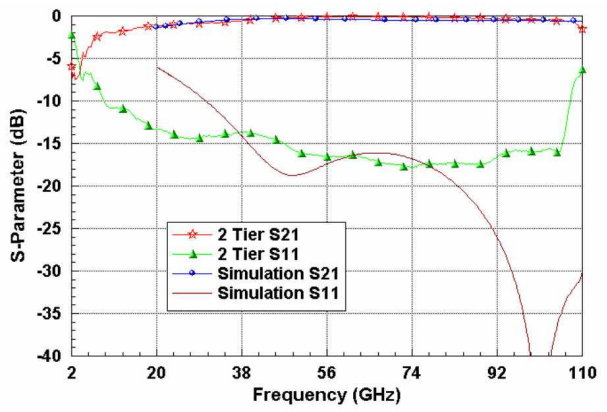



**Figure 2:** Measured and simulated results versus frequency for W-band via-less CPW RF probe pad to microstrip transition

is less than 0.2 dB.

## *1.3 Cantilever Beam RF MEMS Switch Background*

One of the first MEMS devices developed for microwave applications was the switch. An air-bridge type electrostatically activated switch that uses a very high capacitance variation and has very small loss, but a high actuation voltage, has been demonstrated [3]. Switches with serpentine and cantilever springs that exhibit low pull-down voltages, small loss, and good isolation, as well as DC contact MEMS switches [22] and thermally actuated switches have also been demonstrated [8]. The packaging of MEMS switches with liquid crystal polymer (LCP) was also reported [23].

Compared with PIN diodes and FET transistors, RF MEMS switches have very good performance up to approximately 110 GHz, regarding power consumption, linearity, insertion loss, isolation, and bandwidth. They are reliable (more than 40 billion cycles measured), and their performance is degraded only because of the long switching times and the high actuation voltage needed to bias them. The actuation voltage vs. different physical parameters for the cantilever type of switch is shown in Equation (1). The condition of pull-down occurs when the electrostatic attractive (downward) force and the linear restoring (upward) spring force are equal, as in [24].

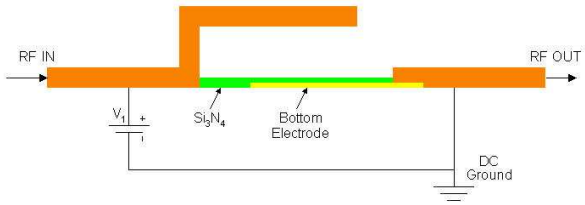



**Figure 3:** The cross setion of cantilever capacitive RF MEMS switches

$$V_s = \sqrt{\frac{8K_{eff}h_{up}^3}{27\epsilon_0 A}} \tag{1}$$

Where $K_{eff}$ is the effective spring constant of the cantilever beam. Given the pull down electrode length of L, the beam width of W, the pull down electrode area A is $A = L * W$, E is Young's modulus for the membrane material, t is the thickness of the membrane, $h_{up}$ is the electrode separation when the membrane is up, and $\epsilon_0$ is the permittivity of the vacuum. This voltage also determines the minimum distance between the biasing lines according to the breakdown voltage of the substrate material. The bias lines were placed at a distance that withstands a voltage of more than 5 times higher than the voltage used.

In my research work, the cantilever beam switch was chosen based on its ease of fabrication and much lower pull down voltage, since it has only one free end compared to the air-bridge type of MEMS switches. The disadvantage of this type of switch is that it is more prone to stress, which may eventually cause a deformation in its shape. One way to solve this problem is to make the beam as short and as thick as possible. However, if the beam is too short or too thick, it will be too stiff, which will lead to an increase of the actuation voltage. Therefore, the trade-off between these parameters should be considered when the MEMS switches are utilized in RF circuits.

The cross sections of these two types of RF MEMS switches are shown in Figure 3 for the cantilever beam capacitive RF MEMS switch, and in Figure 4 for the cantilever beam DC contact RF MEMS switch.

Figure 3 shows the cross section of a cantilever capacitive MEMS switch. As it can be seen, the output "RF OUT" in Figure 3) transmission line is in direct (DC) contact with the bottom electrode,which is covered with a thin film dielectric material such as $Si_3N_4$

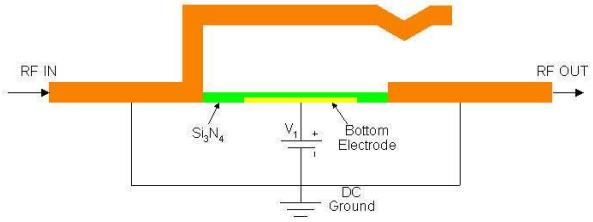



**Figure 4:** The cross setion of cantilever DC contact RF MEMS switches

(Silicon Nitride). Thus, when a voltage ("$V_1$ in Figure 3) is applied between the suspension cantilever beam (or membrane) and the bottom electrode, the membrane will be pulled down. As a result, a very large capacitance will be presented to the RF line, so that the RF signal will go through. This state is called as"on-state" throughout the dissertation. However, when there is no voltage applied ("$V_1 = 0$ in Figure 3) between the membrane and the bottom electrode, the MEMS switch will present a very small capacitance to the RF line, and this case is called as "off-state" of the MEMS switch in the dissertation.

Figure 4 shows the cross section of the DC contact MEMS switch, it has three sections of metals: the first one is the suspension beam (or membrane), the second one is the output transmission line ("RF OUT" in Figure 4), and the last one is the bottom electrode underneath the thin film dielectric material $Si_3N_4$. The operation of this switch is the similar as for the capacitive switch; the difference is that when a voltage is applied between the membrane and the bottom electrode, the membrane will be in DC contact with the output transmission line ("RF OUT" in Figure 4). As a result, it presents a very small resistance, around $0.5 \sim 1\ \Omega$ to the RF line. Figure 4 also shows that there is a small dimple at the end of the suspended cantilever beam, which is formed in the fabrication process, with the purpose of creating a better contact point, as well as to minimize the potential dielectric charging problem of the MEMS switches. Similar to the cantilever capacitive MEMS switch, when it's at the off-state, it will have a very small capacitance, which blocks the RF signal from going through the RF MEMS switch.

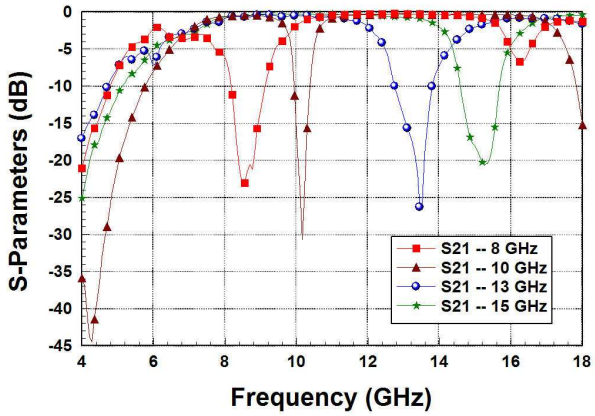



**Figure 5:** Measured composite results of the monolithic reconfigurable bandstop filter with RF MEMS switches.

## *1.4 Reconfigurable Bandstop Filter Background*

The X-band reconfigurable bandstop filter was designed to suppress the spurious and image signals for wireless communication systems and radar systems [25]. The initial design of the bandstop filter is to use quarter-wave length open-circuited resonators [26]. Utilizing the cantilever capacitive RF MEMS switches, a monolithic, low power reconfigurable bandstop filter operating at 8, 10, 13, and 15 GHz has been developed on a high resistivity silicon substrate. The filter is based on the microstrip transmission lines with radial stubs that provide different reactances at different resonant frequencies. The selection of the desired stub reactance is achieved with the cantilever capacitive RF MEMS switches that are electrostatically actuated. The tuning range of the fabricated filter is 7 GHz (8-15 GHz), which is about 60% of the mid-band frequency. The rejection at the notch of the filter and the -10 dB bandwidth range from -20 dB to -27 dB and 5% to 9.7%, respectively. The passband insertion loss was found to be around 0.5 dB.

Figure 5 shows the composite response of the tunable bandstop filter at four different frequencies. The filter will have a notch at a specific frequency when a particular combination of the RF MEMS switches is electrically selected.

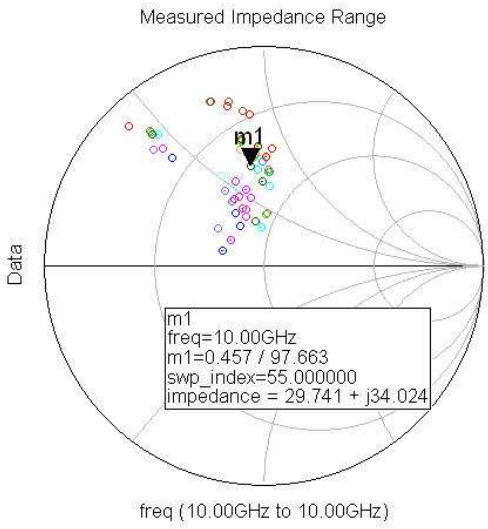



**Figure 6:** Measured 64 impedances of impedance tuner using RF MEMS switches.

## *1.5 Reconfigurable Impedance Tuner Background*

The reconfigurable impedance tuner was designed based on a microstrip transmission line double stub tuner [26]. By using the DC contact RF MEMS switches, each stub in the original tuner was split into three sub-circuits with one MEMS in each sub-circuit. This approach gives a total of 64 different impedances since each switch has two states. By choosing different combinations of the RF MEMS switches, we are able to generate different impedances at the output of the tuner, which are used to provide the conjugate match to the output impedances of the class-E power amplifier. This way, when any external condition changes, such as current drift or temperature variation, which will result in the changes of the output impedances of the power amplifier, the tuner will be able to keep track of these changes to maximize the output power efficiency. The measured tuner loss is approximately 1.5 dB and the measured tuner impedance range is shown in Figure 6. As is shown in Figure 6, the measured impedance range of the tuner is from 3.7 to 45.8 Ω for the real part, and 5 to 44 Ω for the imaginary part. The measured maximum VSWR is 40. The nominal impedance is shown in marker "m1" as 29.7 + 34 Ω, which is very close to the nominal impedance of the power amplifier provided by the University of Colorado, which is 34 + j37 Ω.

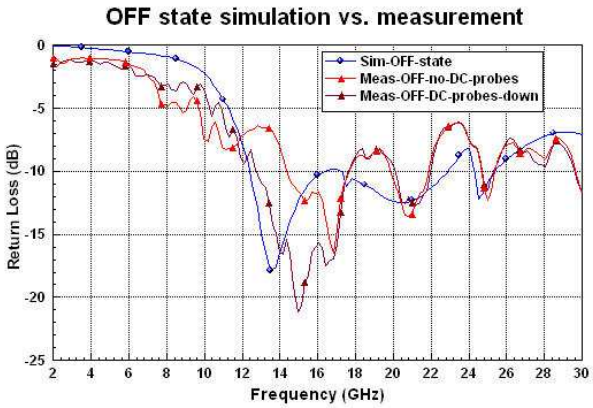



**Figure 7:** Measured and simulated return loss vs frequency for reconfigurable antenna when all switches are at off-state.

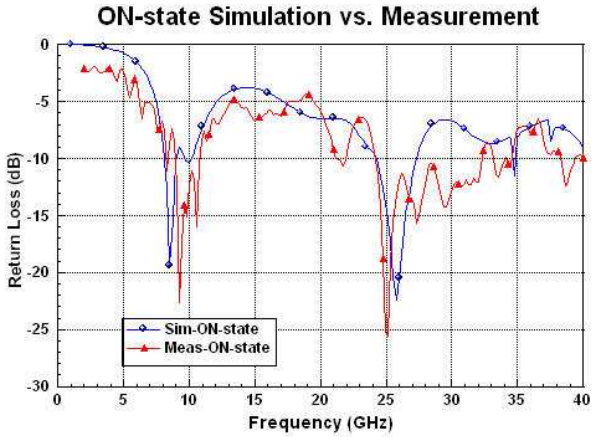



**Figure 8:** Measured and simulated return loss vs frequency for reconfigurable antenna when all switches are at on-state.

## *1.6 Reconfigurable Fractal Antenna Background*

Reconfigurability in an antenna system is a much-desired characteristic that has been the focus of much research in recent years [27]. In this project, the cantilever DC contact RF MEMS switches are integrated with the self-similar planar antennas to provide a reconfigurable antenna system, that radiates with similar patterns over a wide range of frequencies. Various issues regarding the integrations of the antenna with the MEMS switches and the DC bias lines are discussed. Measurements were performed using an Agilent 8510C vector network analyzer for s-parameter extraction. Figures 7 and 8 show the measured and simulated return loss.

Figure 7 shows the return loss of the reconfigurable antenna, when all the switches are at the off-state, with the resonant frequency at 14 GHz. Figure 8 shows the return loss when all the switches are at the on-state. It has two resonant frequencies, the first one is at 8 GHz, and the second one is at 25 GHz. In both cases, the simulated results agree very well with the measured results.

# CHAPTER II

# VIA-LESS CPW RF PROBE PAD TO MICROSTRIP TRANSITIONS

As the demand for high density and high performance microwave and millimeter wave circuits increases, RF devices become smaller and more highly integrated. Often these devices are fabricated with different type of transmission lines. One of the most commonly used transmission lines in RF circuit design is the microstrip transmission line, due to its compact size, ease of fabrication and low cost. However, low cost, rapid characterization of microwave integrated circuits currently requires coplanar waveguide (CPW) probe pads. Thus, a transition from CPW probe pads to microstrip line is required. In order to achieve the highest possible integration, while maintaining each circuit's effective performance, transitions are needed to reduce the mismatch and coupling between different circuit elements. In [28–30] via-less transitions based on radial stubs and sections of coupled lines were developed. These transitions typically require an extensive design process and are not compact for frequencies below 30 GHz. The transitions with via holes have also been developed [31].

This dissertation presents design guidelines for the development of a compact, wideband transition from a coplanar waveguide (CPW) probe pad to microstrip line, that does not require any connection (vias) between the CPW ground strips and the microstrip backside ground plane, and it is also simple to design. The transition was designed and fabricated on a silicon substrate with a center frequency of 20 GHz. The Method of Moments (MoM) was used to both verify the experimental results and optimize the design.

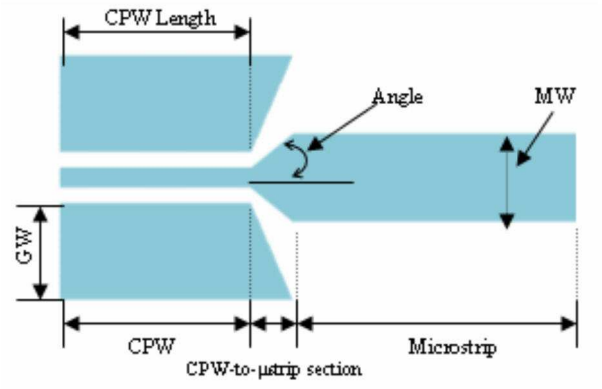



**Figure 9:** Top view of the CPW to microstrip transition structure requiring no vias (bottom ground plane everywhere)

## *2.1 Broad Band Via-Less CPW RF Probe Pad to Microstrip Transition*

### 2.1.1 Transition Design

Figure 9 shows the schematic of the CPW RF probe pad to microstrip transition [32]. This picture has been shown in Chapter 1, but it is shown here again to better describe how this transition works.

The complete structure of the transition consists of a CPW section, a CPW-to-microstrip transition section, and a microstrip section. In the intermediate transition section, the width of the CPW signal strip is gradually increased to match the width of the microstrip. At the same time, the gap between the ground planes and the signal line is widened to retain a 50 Ω characteristic impedance in order to match that of the microstrip line, and minimize reflections. As shown in Figure 9, 'GW' is the width of CPW ground plane width, 'MW' is the width of the microstrip line which is 460 $mu$m to obtain a 50 Ω impedance. The substrate is high resistivity silicon with $\epsilon_r = 11.7$, $\rho > 8000$ Ω - cm, and a thickness of 400 $\mu$m. A thin layer of $SiO_2$ of 1 $\mu$m thick was deposited on the silicon wafer as an insolation layer prior to the circuit fabrication. The signal line width of the CPW is 104 $\mu$m while the slot (gap) width is 80 $\mu$m. In order to better understand this transition and derive some design guidelines, the CPW section length ('CPW Length' in Figure 9) and angle ('Angle' in Figure 9) of the transition between the CPW and microstrip were studied and varied. The length of the intermediate section can be calculated from the chosen angle.

The length of the CPW section was chosen so that it's long enough to make sure the CPW mode will build up along the line, as well as it's short enough to maintain the compact size. The center signal width of the CPW section was gradually changed to the signal width of the microstrip transmission line, which will make sure that the CPW mode will gradually change to the microstrip mode. A sharp change (ie. straight tapper) will cause a large discontinuity between these two sections, thus, the transition performance will degrade. The last section of the transition is the 50 Ω microstrip transmission line.

High resistivity silicon wafers were used to prevent the energy leakage through the substrate; the thickness of 400 $\mu$m of the substrate and the excitation mechanism (RF CPW probes) also contribute to the minimization of the presence of the microstrip mode in the coplanar section [33]. The same substrate was later used for reconfigurable microwave circuit development. Furthermore, by choosing each of the ground plane width of the CPW section much smaller than $\lambda_g/4$ ($\lambda_g$ is the transmission line guided wavelength), the parallel plate and other higher order modes can be minimized or avoided [34].

### 2.1.2 Simulations and Measurements

Full wave simulations for various combinations of geometrical parameters were performed, by using Agilent Momentum to reduce the insertion loss, and optimize the design in terms of the size and the operating bandwidth. To facilitate the on-wafer measurements, each structure was fabricated as two CPW-to-microstrip transitions with a back-to-back configuration. In order to compare on the same basis with the simulated results, one half of the insertion loss (dB) was deducted from the measured results and compared with the simulated results. It should be noted here that the measured results can not be compared to the simulations as "apple to apple", since simulations were done on one transition instead of two with a back to back configuration. A more accurate method was used to better compare the results between the simulations and measurements for a W-band transition development.

The fabrication was done on a high resistivity silicon wafer mentioned above. Since this is a single-layered fabrication process, it's fairly easy compared with the multi-layered

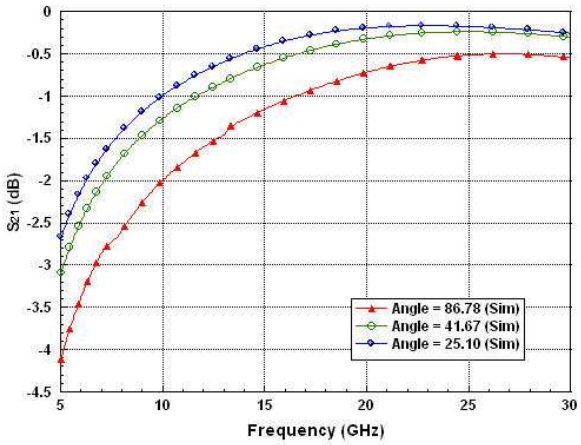



**Figure 10:** Simulated insertion loss vs. frequency for different transition angles

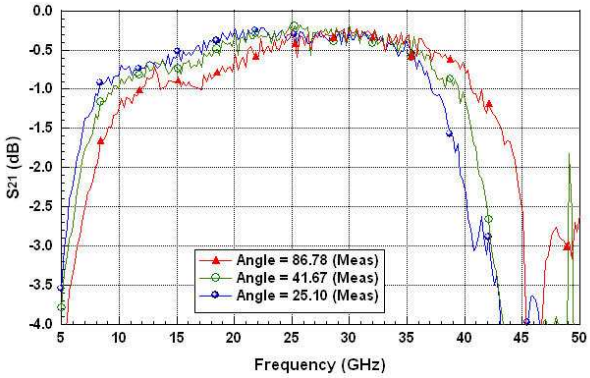



**Figure 11:** Measured insertion loss vs. frequency for different transition angles

fabrication process for reconfigurable microwave circuits using RF MEMS switches. The metallization layer for the transmission lines is 3 $\mu$m thick of electro-plated gold, which is sufficient to prevent any conductor loss due to the skin effect. The gold was also electro-plated everywhere on the backside of the substrate, to provide the ground plane for the microstrip transmission lines. The measurements were performed with an Agilent 8510C vector network analyzer, and the calibration was done with the SOLT method. The detailed fabrication process can be found in Appendix I.

The measured and simulated results with respect to different transition angles and CPW lengths are shown in the following Figures 10 to 15.

Figure 10 displays the simulated loss from 5 to 30 GHz for the transition, with the

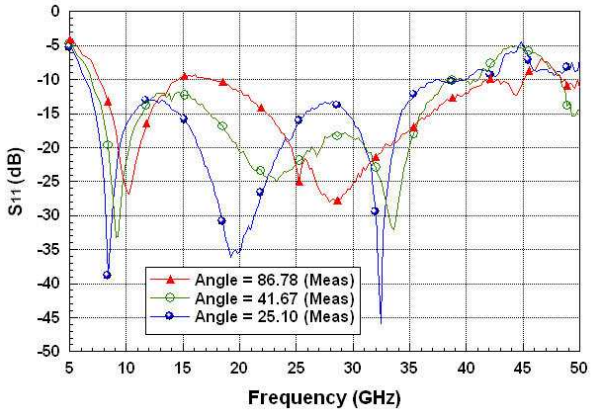



**Figure 12:** Measured return loss vs. frequency for different transition angles

design angles varying from 25.1° to 86.7°. For this experiment, the 'GW' and CPW length in Figure 9 were fixed to be 800 $\mu$m and 400 $\mu$m, respectively. The specific angles were chosen because they correspond to the intermediate section length of 10 $\mu$m, 200 $\mu$m and 380 $\mu$m, for an angle of 86.78°, 41.67° and 25.1°, respectively. As it is shown in Figure 10, when the angle decreases, the transition loss gets smaller. This is expected, since as the angle decreases, the transition between the CPW to microstrip line becomes smoother, thus, the sharp discontinuities are reduced. An angle below 40° is found to be good enough to produce practically the optimum results.

Figure 11 shows the measured insertion loss from 5 to 50 GHz, with respect to the different transition angles. The results were taken as one half of the measured $S_{21}$ for a CPW to microstrip transition with the back to back configuration. The graph shows that the measured and simulated results have a good agreement, and when the angle is around 40° the insertion loss is optimized in terms of the value and bandwidth. More specifically, with this angle the loss is below 1 dB from 10 to 40 GHz, and with a value of 0.4 dB at 20 GHz. The 3-dB bandwidth is 185%. For the smaller angles, the difference in the transition loss is very small, but the bandwidth performance deteriorates. The angle of 41.67° was chosen as the nominal value for further investigation of this transition.

Figure 12 shows the measured return loss for the different transition angles. It can be observed, that the return loss is optimized for the smallest angles, as expected, and that for a angle of 41.67°, the return loss is better than 12 dB from 7 to 37 GHz.

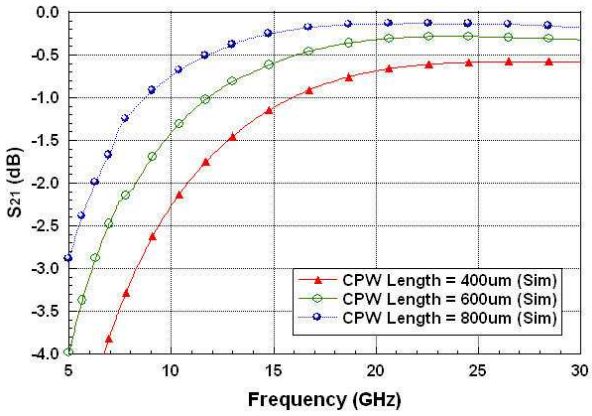



**Figure 13:** Simulated insertion loss vs. frequency for different CPW section lengths

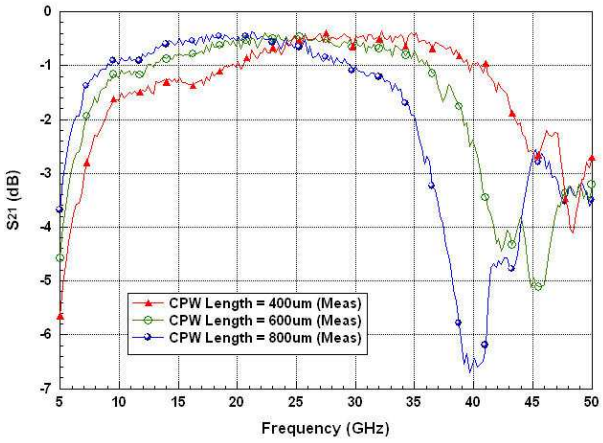



**Figure 14:** Measured insertion loss vs. frequency for different CPW section lengths

Figure 13 shows the simulated insertion loss for different CPW lengths as defined in Figure 9, and for a transition angle of 41.67°. The width 'GW' was chosen to be 500 $\mu$m, to reduce the total size of the structure and also reveal the effect of the finite ground plane. As it can be seen, when the CPW length changes from 400 $\mu$m to 600 $\mu$m and then to 800 $\mu$m, the transition performance improves when the CPW length increases.

Figure 14 is a plot of the measured insertion loss from 5 to 50 GHz, with respect to the different CPW section lengths. It clearly shows that from 5 to 25 GHz, the insertion loss decreases as the CPW section length increases, and when the frequency is above 25 GHz the opposite effect occurs. For a length of 600 $\mu$m, the insertion loss is less than 1 dB from

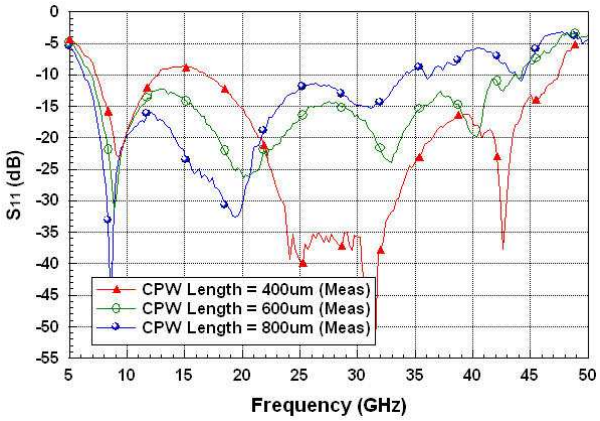



**Figure 15:** Measured Return loss vs. frequency for different CPW section lengths

12 to 36 GHz, with a value of 0.5 dB at 20 GHz. Taking into account the effective dielectric constant for the CPW section, it was found that the line length of 400 $\mu$m, 600 $\mu$m and 800 $\mu$m corresponds to 0.067 $\lambda_g$, 0.1 $\lambda_g$ and 0.133 $\lambda_g$ at 20 GHz, respectively. This shows that in order to get an optimum insertion loss for the frequency of interest, the CPW length needs to be around 0.1 $\lambda_g$. This allows the coplanar mode to build-up and is the best compromise for the optimum loss and bandwidth. Comparing Figures 11 and 14, it can be seen that the former graph shows a slightly smaller insertion loss. This is expected since the CPW ground plane size is reduced to 500 $\mu$m from 800 $\mu$m for the latter study, which results in a higher current density at the CPW ground strips and a smaller total capacitance from the CPW ground plane to microstrip ground plane. Thus, the electrical reactance X between the CPW probe ground and microstrip ground increases, in other words, the impedance between the CPW probe ground and microstrip ground increases slightly [30].

Figure 15 shows the measured return loss for the transition with the different CPW lengths. As it is seen, the return loss is optimum with respect to both the value and the bandwidth, when the CPW length is 600 $\mu$m. With this length, the return loss is better than 13 dB from 7.5 to 42 GHz, and a return loss of 26 dB was measured at 20 GHz. For a longer length (800 $\mu$m), the return loss is larger than 11 dB from 7 to 34 GHz.

### 2.1.3 Conclusions

To conclude this section, a CPW RF probe pad to microstrip transition has been presented. This transition does not require any vias between the CPW ground planes and the microstrip backside ground plane; therefore it simplifies the fabrication and lowers significantly the production cost. The measurements showed that an insertion loss of 0.4 dB can be achieved at 20 GHz, and it is below 1 dB from 10 to 40 GHz for an angle around 41°. In addition, the CPW length should be approximately 0.1 $\lambda_g$ at the design frequency for the optimum result. To the authors' knowledge, this is the smallest reported loss with the widest bandwidth ($\sim$ 185%) for such a compact and via-less transition.

Future work involved in this area is to extend the transition to different frequency ranges, as discussed in the next section for a W-band transition.

## *2.2 W-Band Via-Less CPW RF Probe Pad to Microstrip Transition*

The design rules for the CPW RF probe pad to microstrip transition were established in the above section, by studying multiple transitions centered at 20 GHz on a 400 $\mu$m thick high resistivity ($\rho > 8000$ $\Omega$ - cm) silicon wafer. This section presents a via-less CPW RF probe pad to microstrip transition that demonstrates the effectiveness of these design rules at W-band, along with a more robust measurement technique [35]. As compared with [28–31], this transition is simpler, more compact and more broadband, which covers the frequency range from 20 GHz to 100 GHz.

The W-band transition was designed and fabricated on a 100 $\mu$m thick high resistivity ($\rho > 8000$ $\Omega$-cm) silicon wafer, with a center frequency of 70 GHz. The Method of Moments (MoM) was used to both verify the experimental results and optimize the design.

### 2.2.1 W-band Transition Design and Fabrication

Figure 16 shows the schematic of a coplanar waveguide (CPW) to microstrip transition. The complete structure consists of a CPW section, a CPW-to-microstrip transition section, and a microstrip section, which is the same as in the previous section. In the intermediate

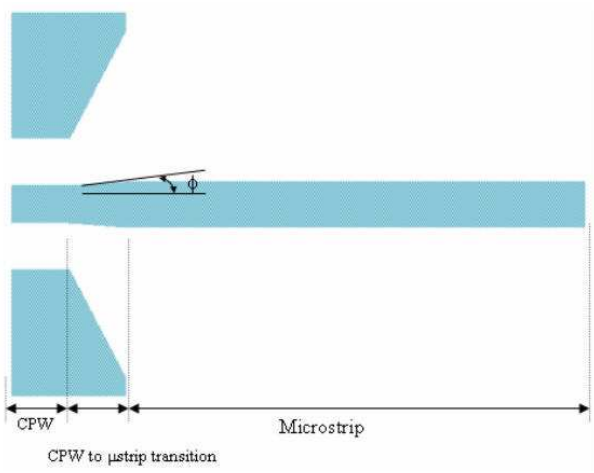



**Figure 16:** Top view of the W-band CPW to microstrip transition structure requiring no vias (Bottom ground plane everywhere)

transition section, the width of the CPW signal strip is gradually increased to match the width of the microstrip line. The "$\phi$" in Figure 16 shows the angle between the CPW signal line and the microstrip line. At the same time, the gap between the ground planes and the signal line of the CPW section is gradually widened to retain a 50 Ω characteristic impedance, in order to match that of the microstrip line, and minimize the reflections and parasitic effects.

The W-band transition is designed with a center frequency of 70 GHz and built on a 100 $\mu$m thick high resistivity silicon wafer, with $\epsilon_r = 11.7$, and $\rho > 8000$ Ω-cm. Compared to the previous section, a much thinner silicon wafer was chosen in order to avoid the higher order mode excitation at higher frequencies. The metallization layer is electro-plated gold with a thickness of 3 $\mu$m, which provides sufficient conductor thickness at both lower (X-band) and higher (W-band) frequencies. The back side of the wafer is metallized to provide the ground plane for the microstrip transmission lines.

The dimensions of the transition are as follows [35]: for the CPW section, the signal line width is 90 $\mu$m; the gap between the CPW signal line and ground strips is 110 $\mu$m. These two values give the CPW section a 50 Ω characteristic impedance with the given substrate information. The length of the CPW section and the transition section is 100 $\mu$m, which is around 0.07 $\lambda_g$ at 70 GHz, and 0.1 $\lambda_g$ at 100 GHz. The width of the transition is gradually

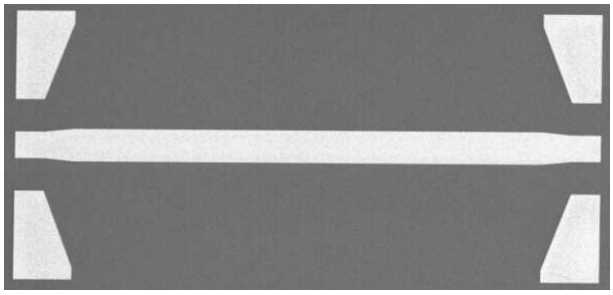


**Figure 17:** SEM picture of two CPW to microstrip transition with back-to-back configuration

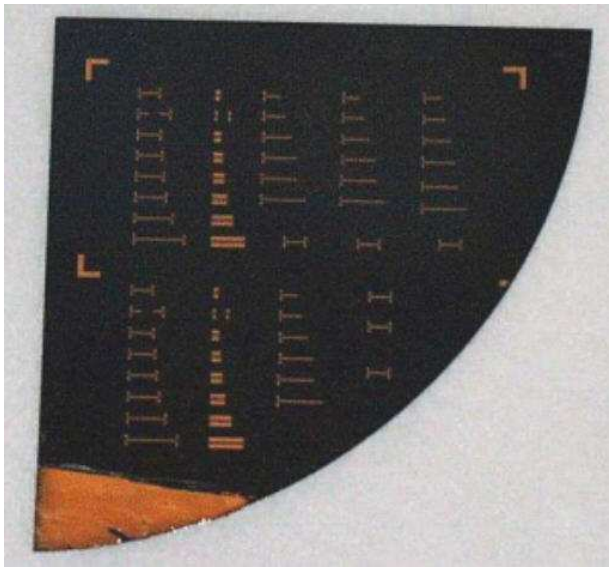


**Figure 18:** Picture of fabricated CPW to microstrip transitions with TRL, conductor backed CPW and microstrip stub standards

changed from 90 $\mu$m (the CPW line width) to 110 $\mu$m (the microstrip line width). The corresponding angle "$\phi$" is 5.7°. The fabricated circuits are shown in Figures 17 and 18. The detailed fabrication process is the same as in the previous section, which can be found in Appendix I.

Figure 17 shows the SEM picture of two CPW to microstrip transitions with a back to back configuration. Figure 18 shows the picture of the fabricated circuits on a quarter piece of a 4" silicon wafer, with the CPW probe pad to microstrip transitions and different sets of calibration lines.

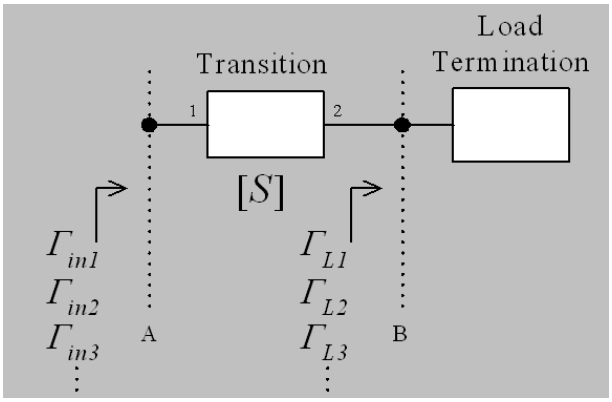



**Figure 19:** Measurement configuration for the unterminating technique for an on-wafer measurement of transition

### 2.2.2 Deembedding and Measurements

Two different measurement methods were chosen to accurately determine the S-parameters of the transition: an unterminating technique similar to that in [36] and a two-tier deembedding technique using NIST's Multical Software [37]. For calibration purposes, a CPW calibration and a microstrip calibration set were fabricated containing 6 delay lines to cover 20-110 GHz. The measurements were performed using an Agilent 8510XF and GGB 110H Picoprobes.

The procedure for the unterminating technique uses the measurements made at the input of an unknown 2-port network (the embedding network, in this case the transition), with different 1-port load terminations (in this case the microstrip stubs with differing length) at its output as shown in Figure 19.

The known load terminations are connected at the output port (port 2) of the transition whose characteristics are desired. This connection point is labeled as plane B in Figure 19; it is also the plane at which the characteristics of the terminations are known, specifically their reflection coefficients $\Gamma_L$ at each measurement frequency. The measured reflection coefficients at plane A, $\Gamma_{in}$, are related to the known reflection coefficients produced by the $i_{th}$ termination at plane B, by the scattering matrix that defines the unknown passive transition network as in (2):

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{2}$$

This technique requires a minimum set of three measurement pairs to solve for $S_{11}$, $S_{22}$, and the product $S_{12}S_{21}$. However, to reduce the measurement related errors, redundant terminations can be used in order to obtain an average over the solutions of the calculated S-parameters. If reciprocity can be assumed for the unknown network, the transmission coefficients $S_{21}$ and $S_{12}$ are equal and can be obtained from the product $S_{12}S_{21}$. There is an ambiguity, however, on the sign of $S_{21}$, which can simply be resolved by making a delay measurement of the network.

For the unterminating technique, six identical transitions were used with the microstrip open stubs (load termination) of differing lengths attached to the end of the transition (see Figure 19). In order to ensure the proper calibration NIST's Multical [37] was used, establishing the CPW reference plane at the probe tips (reference plane A, Figure 19) and the microstrip reference plane after the transition (reference plane B, see Figure 19) to characterize each microstrip stub. The six terminations (stubs) were characterized using the microstrip calibration. Subsequently the input reflection coefficient was measured for each transition and termination pair using the CPW calibration. Using all six measurement pairs, taken three at a time, twenty solutions for the S-parameters of the transition were obtained at each frequency. The S-parameters of the transition were then obtained by averaging over all of the measurements.

The two tier deembedding technique utilizes the same calibrations sets (the CPW and microstrip) as in the unterminating technique. The result gives the S-parameters of the transition used in the microstrip calibration set. A comparison of the two techniques is shown in figures 20 and 21.

The results show a very good agreement between the two different techniques. As shown in Figures 20 and 21, the 1-port unterminating method is more prone to the measurement and probing errors than is the two-port two-tier method. Additional measurements can increase the accuracy and reduce the residual error present in the results.

The measured results are compared with the simulated results (Agilent Momentum) in

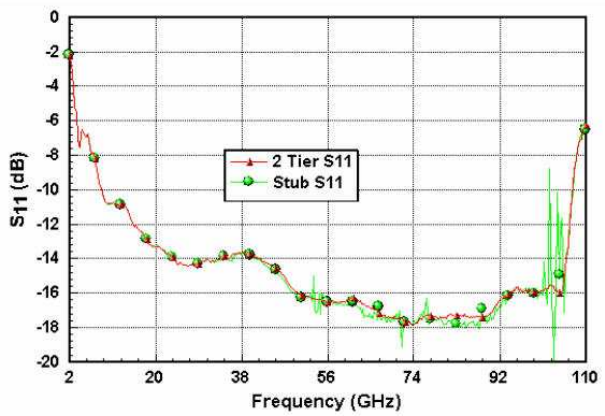



**Figure 20:** $S_{11}$ comparison of the CPW to Microstrip transition using the 2 tier deembedding and unterminating technique

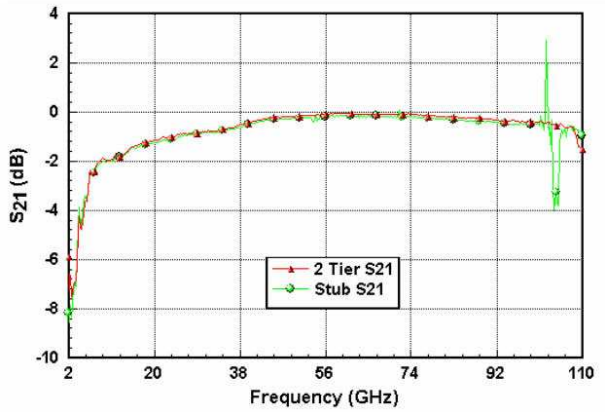



**Figure 21:** $S_{21}$ comparison of the CPW to Microstrip transition using the 2 tier deembedding and unterminating technique

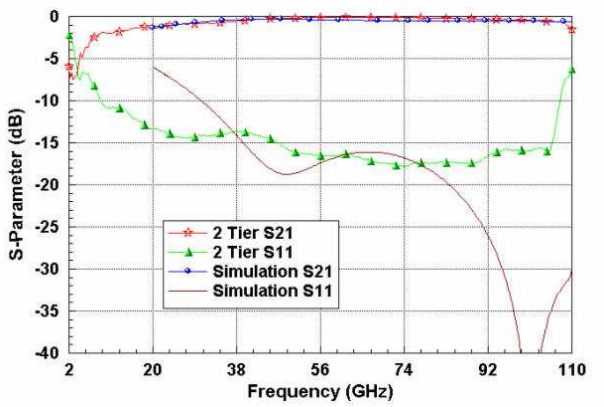



**Figure 22:** $S_{21}$ comparison of the CPW to Microstrip transition using the 2 tier deembedding and unterminating technique

Figure 22.

Figure 22 shows that the measured and simulated insertion loss agrees very well from 20 GHz to 100 GHz, with an average loss about 0.4 dB, while from 50 GHz to 80 GHz, the insertion loss is less than 0.2 dB. From 100 to 110 GHz range, the measurement shows a sharp rise for $S_{11}$, which is probably due to a higher order excited at this frequency range.

### 2.2.3 Conclusions

This section presents a wideband CPW probe pad to microstrip transition for the W-band frequency range. This transition does not require any connection (vias) between the CPW ground planes and the microstrip backside ground plane; therefore, it simplifies the fabrication and lowers significantly the production cost. Two measurement methods showed that a loss of 0.4 dB is achieved from 40 GHz to 100 GHz, with a 3- dB bandwidth of $\sim$173%. This transition can be used in testing of a variety of RF/millimeter wave systems due to its broad bandwidth and low loss.

# CHAPTER III

# RF MEMS SWITCHES REVIEW

RF MEMS switches have become one of the fast emerging technologies in recent years due to their superior RF performance. Intensive research studies have been conducted to explore the performance of RF MEMS switches, as well as reconfigurable RF/microwave circuits using MEMS switches [2–4, 38]. MEMS switches have a very small size and their fabrication process is CMOS compatible, so, they can be easily integrated with the rest of the circuitry. They have exhibited extremely low loss for up to 110 GHz, as shown in the recent research reports [39, 40]. They almost don't consume any power, and they are easy to actuate. Since RF MEMS switches have demonstrated an excellent linearity over a wide frequency band, they present very low distortion to the communication systems. In contrast, for the traditional switching devices or tuning elements, such as PIN diodes, FET transistors or varactors, they will add more loss to the circuitry at higher frequencies, and introduce non-linear effects to RF/microwave communication systems. The MEMS varactor is another alternative tuning device for the reconfigurable microwave circuits, but because of the limitation of its smaller tuning range, it can not provide a tuning range as wide band as the MEMS switch. Thus, MEMS varactors are not suitable yet for wide band tunable microwave circuitry.

However, RF MEMS switches also have some challenging issues that have to be addressed, before being widely adopted in the commercial sector. The most important issue is the RF MEMS switch packaging, which has been identified as one of the most significant research areas of enabling RF MEMS switches as real life products. Extensive studies have been done both in academic institutions and companies in this area [41–45]. To maintain the superior RF performance, the MEMS switch needs a hematic or a near hematic package which will protect it from the environment. The un-packaged RF MEMS switch will experience RF performance degradation, and show stiction problems. Thus, a hermetic or near

hematic, as well as low loss packaging material must be provided to maintain the excellent RF performance of the MEMS switches.

Liquid crystal polymer (LCP) is a new material that has been identified as a very good candidate for the MEMS switch packaging, due to its near hermetic nature, low loss at RF/microwave frequencies, and moldability. A recent research has been reported in this area [23].

MEMS switches also have some other non-significant problems, which are shown as follows: First, they can not handle as much RF power as PIN diodes, FET transistors or varactors; Second, their switching time is relative longer. The switching time of MEMS switches varies from 1 $\mu$secs to 30 $\mu$secs, while the PIN diodes or the FET transistor switch are in nano-second ranges; Third, MEMS switches potentially have dielectric charging problems, which could be minimized using an appropriate actuation scheme. The different topologies of MEMS switches and different fabrication processes have been studied to resolve this problem [1, 46]; Last, MEMS switches require higher actuation voltages compared to PIN diodes or FET transistors. The research reports show the actuation voltage varies from 5 volts to 90 volts [1, 3, 9, 25].

Many different types of MEMS switches have been developed [3, 4, 7, 9]. In this dissertation, the cantilever type of MEMS switches were used for reconfigurable microwave circuit design and development. Compared to air-bridge MEMS switches, the main advantage of cantilever MEMS switches is they have much lower actuation voltage. Two types of cantilever RF MEMS switches are presented in this chapter: one is the cantilever capacitive MEMS switch, and the other one is the cantilever DC contact MEMS switch.

## *3.1 Cantilever Capacitive RF MEMS Switches*

Cantilever beam capacitive RF MEMS switches were used in the reconfigurable bandstop filter development [25], because of its ease of design and fabrication. The cross section of this type of MEMS switch is shown in Figure 23.

As shown in Figure 23, the MEMS switch has a suspension beam (membrane) connected to the input transmission line ("RF IN" in Figure 23), and a bottom electrode connected to

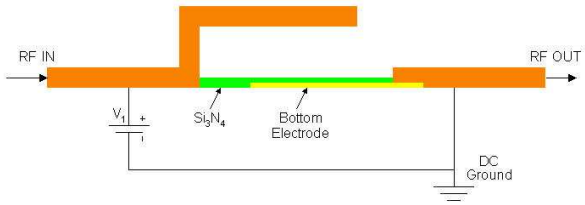



**Figure 23:** The cross section of the cantilever beam capacitive MEMS switch

the RF output transmission line ("RF OUT" in Figure 23). The bottom electrode is covered by a thin layer (2000 $\mathring{A}$) of silicon nitride ($Si_3N_4$). The suspension beam has one free end, thus, it requires a lower actuation voltage compared to a similar air bridge MEMS switch (given the same overlap area and the same suspension distance between the membrane and the bottom electrode).

Also as shown in Figure 23, a voltage "$V_1$" is connected between the input transmission line and the output transmission line, or, $V_1$ is applied between the membrane and the bottom electrode. This connection shows the actuation method of the capacitive MEMS switch. When $V_1$ is 0, the membrane will be at the up position, or the MEMS switch at the off-state, the RF signal will be blocked from going through the switch since it shows a capacitive open. When a voltage (positive or negative) is applied between the membrane and the bottom electrode, or when $V_1 \neq 0$, the membrane will be pulled downward. When $V_1$ is large enough and equals to the spring force of the membrane, the membrane will be pulled down and create a contact with the dielectric material ($Si_3N_4$) on top of the bottom electrode, thus, a capacitive short will be created. This is called the "on-state" of the MEMS switch, and the voltage applied is called the actuation voltage.

For the cantilever MEMS switch, the actuation voltage can be calculated from Equation (3):

$$V_s \cong \sqrt{\frac{8K_{eff}h_{up}^3}{27\epsilon_0 A}} \tag{3}$$

In equation (3), $K_{eff}$ is the effective spring constant, $h_{up}$ is the distance between the membrane and the bottom electrode when the membrane is at the up position, and A is the area of the pull down electrode.

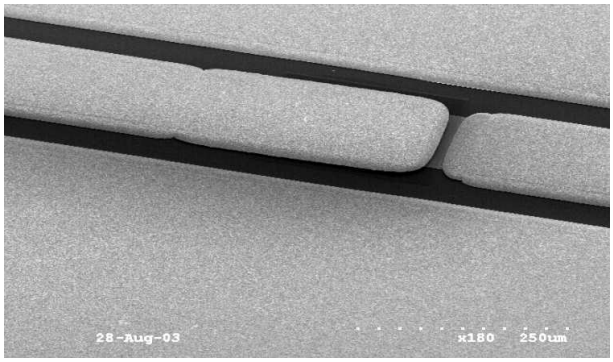



**Figure 24:** SEM picture of a fabricated cantilever capacitive MEMS switch

The cantilever capacitive MEMS switch presented in this dissertation has a beam width of 110 $\mu$m, and a length of 280 $\mu$m; while the overlap area (pull down area) between the beam (membrane) and the bottom electrode was 110 $\mu$m x 100 $\mu$m. The thickness of the membrane is around 2 to 2.5 $\mu$m, and the suspension distance between the membrane and the bottom electrode is around 2 $\mu$m. The actuation voltage calculated from Equation (3) is about 27 volts.

Figures 24 and 25 show the pictures of a fabricated cantilever beam capacitive MEMS switch. Figure 24 shows the MEMS switch with a CPW configuration, which is for the on-wafer probing; while Figure 25 is a close-up of the MEMS switch. As shown in Figure 25, the MEMS switch is constructed with three metals, the membrane, the bottom electrode and the output transmission line. The membrane is suspended on top of the bottom electrode which is covered by a thin layer of $Si_3N_4$. Thus, when the membrane is at the up position, or the MEMS switch at the off- state, the MEMS switch will present a very small capacitance to the RF line, and RF signal will not go through. But when the actuation voltage is applied between the membrane and the bottom electrode, the membrane will be pulled down, and in contact with $Si_3N_4$, as a result, a capacitive short will be created. Thus, RF signal will go through and the RF energy will be delivered to the output transmission line.

The multi-layered fabrication process was developed to complete the fabrication of the cantilever capacitive MEMS swtiches. The detailed fabrication process can be found in Appendix II.

The measurements of the fabricated MEMS switches were done by using an Agilent

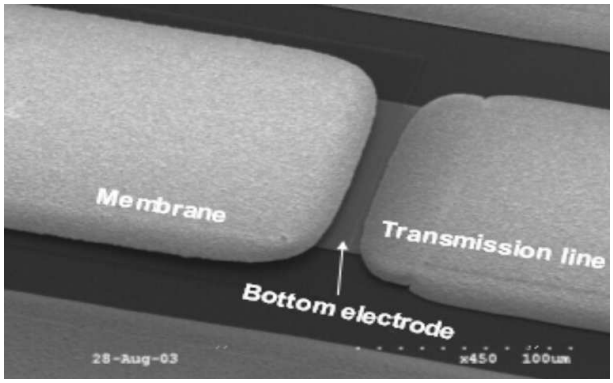



**Figure 25:** SEM close-up of a cantilever capacitive MEMS switch

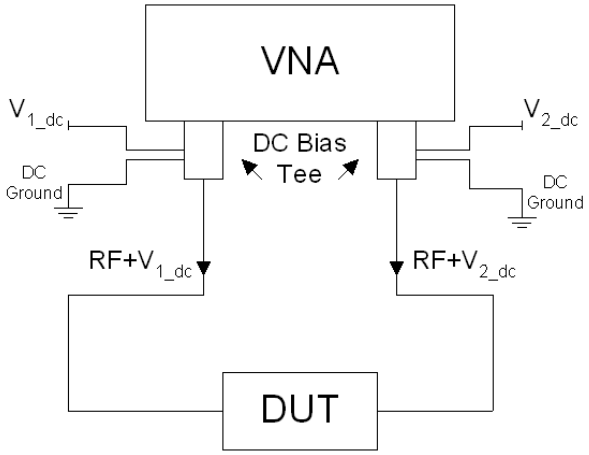



**Figure 26:** Measurement setup for cantilever capacitive MEMS switches

8510C vector network analyzer (VNA) and a Cascade probe station. RF probing was done using GGB RF probes, with a pitch of 150 $\mu$m. The SOLT method was used for the calibration. The actuation voltage for the MEMS switches was applied between the membrane and the bottom electrode, through the RF transmission lines. To realize this, two bias Tees were connected between the VNA and the RF cables (RF cables connect to the RF probes). This setup is shown in Figure 26.

As shown in Figure 26, two bias tees were connected to each port of the VNA, and the other side of each bias tee was connected to the "DUT" (device under test) through the RF cable and the RF probe. Here, the "DUT" is the capacitive MEMS switch in CPW configuration. By applying the voltage to the DC pin of the bias tee, the output of the bias tee contains two signals: the RF signal and the DC voltage ($v_{1_{dc}}$ and $v_{2_{dc}}$ from the output

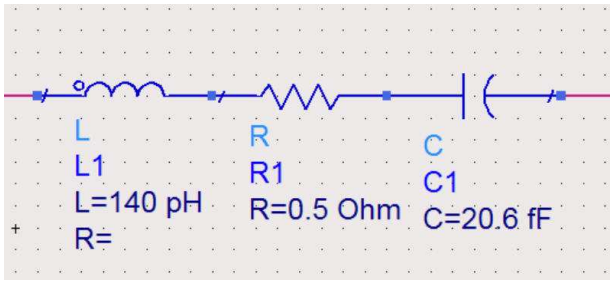



**Figure 27:** Equivalent circuit model of the cantilever capacitive MEMS switch at the off-state

of each bias tee). By choosing either one of them as the DC ground, the other one will be the actuation voltage.

The measured actuation voltage was 35 volts, which is slightly higher than the result from the theoretical calculation. This is because of the variations from the fabrication process. The s-parameters of the MEMS switch were taken, and the measured results were curve-fitted to the simulated results from the MEMS switch equivalent circuit model [1], to extract the off-state capacitance and the on-state capacitance.

The equivalent circuit model of the MEMS switch at the off- state is shown in Figure 27. As it can be seen, when the MEMS switch is at the off- state (the membrane at the "up" position), it is modeled as a very small inductor (140 pH) in series with a small resistor (0.5 Ω) and a capacitor which is around 20 fF $\sim$ 30 fF (several samples of the fabricated MEMS switches were measured). The results from the measurements and simulations are shown and compared in Figure 28.

Figure 28 shows that the simulated results from the circuit model in Figure 27 gives a very good agreement with the measured results. It can be seen from Figure 28, when the cantilever capacitive MEMS switch is at the off-state, it has an isolation of about -20 dB to -15 dB from 8 GHz to 15 GHz, and a return loss about -0.22 dB to -0.45 dB from 8 GHz to 15 GHz.

On the other hand, when the actuation voltage is applied through the bias tee, between the membrane and the bottom electrode, the MEMS switch will be activated (or at the on-state) and exhibit a very high capacitance which is extracted to be around 900 fF $\sim$ 1 pF from the simulations. The equivalent circuit model is shown in Figure 29. As it is shown in

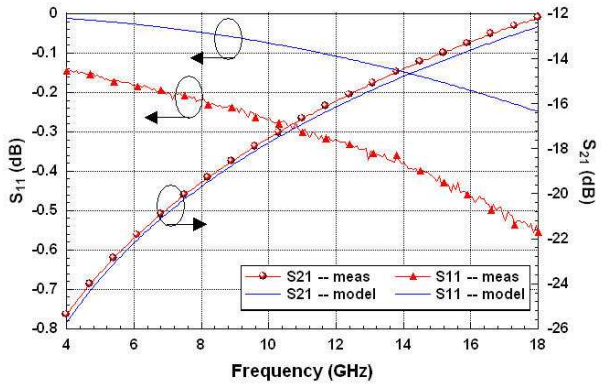



**Figure 28:** Measured vs simulated S-parameters of cantilever capacitive MEMS switch at off-state

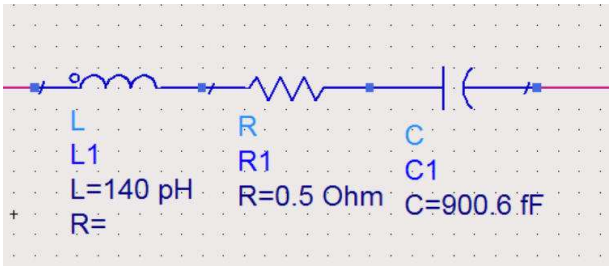



**Figure 29:** Equivalent circuit model of the cantilever capacitive MEMS switch at the on-state

Figure 29, when the MEMS switch is at the on- state, it is modeled as a very small inductor (140 pH) in series with a small resistor (0.5 Ω) and a capacitor which is around 900 fF $\sim$ 1 pF (several samples of the fabricated MEMS switches were measured). The measured and simulated results are shown and compared in Figure 30.

Figure 30 shows that the simulated results from the circuit model in Figure 29 gives a very good agreement with the measured results. As it can be seen from Figure 30, when the cantilever capacitive MEMS switch is at the on-state, it has an insertion loss of about -0.3 dB to -0.15 dB from 8 GHz to 15 GHz, and a return loss of about -17 dB to -35 dB from 8 GHz to 15 GHz.

## *3.2 Cantilever DC Contact MEMS Switches*

The cantilever DC contact MEMS switch was used for an X-band reconfigurable impedance tuner development [47]. Since it is also a cantilever type of MEMS switch, the same equation

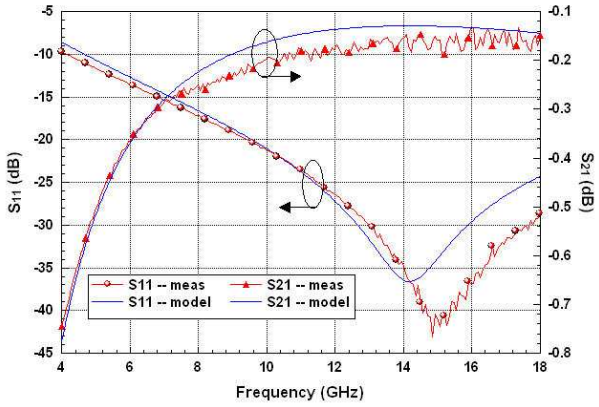



**Figure 30:** Measured vs simulated S-parameters of cantilever capacitive MEMS switch at on-state

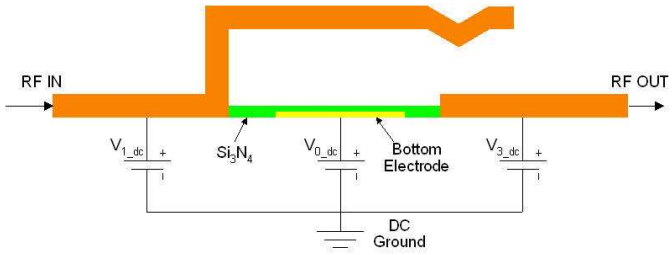



**Figure 31:** The cross section of the cantilever beam capacitive MEMS switch

as in Equation (3) can be used to calculate the theoretical actuation voltage. With the improved fabrication process, it was found that the fabricated DC contact MEMS switch was easier to actuate, and has shown fewer problems, such as stiction and dielectric charging problems, when operated un-packaged. The cross section of the DC contact MEMS switch is shown in Figure 31.

As it is shown in Figure 31, there is a significant improvement in the DC contact MEMS switch: A dimple at the end of the membrane was created in the fabrication process. This has helped to minimize stiction problems and the dielectric charging problems [48], as well as create a better metal contact between the membrane and the bottom contact metal, when the MEMS switch is at the on-state.

The DC contact MEMS switches were fabricated and measured on the same wafer as for the X-band reconfigurable impedance tuner and antenna. The detailed fabrication process can be found in Appendix IV. The fabricated MEMS switch has a suspension distance

between the membrane and the bottom electrode of about 2 $\mu$m, and a thickness of the membrane of about 2 $\mu$m; the width and length of the membrane is 110 $\mu$m and 175 $\mu$m, respectively. With these values, the actuation voltage can be calculated from Equation (3), which is about 25 volts.

The measurement was done using an Agilent 8510C vector network analyzer with GGB RF probes, and a Cascade DC probe. The SOLT method was used for the calibration. The measured actuation voltage is from 25 volts to 35 volts, and switching time measured is around 5 $\mu$secs for an un-packaged switch.

The picture of a fabricated DC contact MEMS switch is shown in figure 32. As can be seen in Figure 32, the fabricated DC contact MEMS switch is in CPW configuration, in order to enable the RF probing. The "DC probe pad" in Figure 32 is connected to the bottom electrode through a highly resistive material AZO (Aluminum doped Zinc oxide), with the sheet resistance around 100 K$\Omega$/square. The AZO DC bias line has a width of 20 $\mu$m, and a length of 400 $\mu$m, so equivalently its length is 20 squares. This gives a total DC resistance of around 2 M$\Omega$, which is sufficient to prevent RF energy leakage from the DC bias lines. AZO is also directly connected to the DC probe pad, which will enable a DC voltage application to the bottom electrode. Figure 32 also shows a second significant improvement of the DC contact MEMS switch over the capacitive MEMS switch: there is a small opening in the membrane, which will decrease the spring force of the membrane, thus, lower the actuation voltage. This opening has also made it easier to remove the sacrificial layer in the fabrication process, when the MEMS switch is being released.

When the DC contact MEMS switch is at the off-state, or when the membrane is at the up position, similar to a capacitive MEMS switch, it exhibits a very small capacitance which will block the RF path. But when the actuation voltage is applied between the membrane and the bottom electrode, the membrane will be pulled down and it will be in DC contact with the bottom contact metal which connects the output transmission line ("RF OUT") as shown in Figure 31. The MEMS switch at the on- state has a very small contact resistance and provides an RF through path.

The actuation mechanism of the DC contact MEMS switch is different from that of

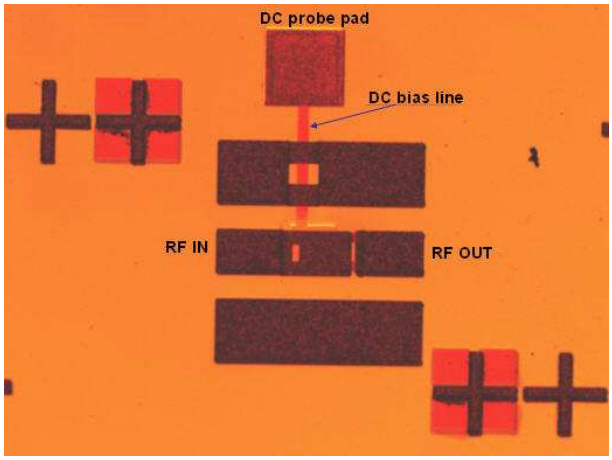



**Figure 32:** Picture of a fabricated cantilever DC contact MEMS switch

the capacitive MEMS switch presented in the previous section. As it is shown in Figure 31, there are three different voltages applied to the MEMS switch, "$V\_0_dc$","$V\_1_dc$", and "$V\_2_dc$". The voltage $V\_0_dc$ connects to the bottom electrode, $V\_1_dc$ connects to the input transmission line or the membrane, and $V\_2_dc$ connects to the output transmission line or the bottom contact metal. Since when the MEMS switch is at the on- state, the membrane will be pulled down and in DC contact with the bottom contact metal, or the output transmission line, the bottom electrode can't be connected to the output line, in another words, $V\_0_dc$ has to be different from $V\_2_dc$. Otherwise, it will create a short circuit at the output of the DC supply, which will destroy the MEMS switch or even the VNA due to the high current. Hence, a separate DC probe pad must be provided to connected to the bottom electrode as shown in Figure 32. For a proper actuation, the same potential should be provided between the membrane and the bottom contact metal to avoid any possible electro-static shot. So, in summary, there are totally three connections for the DC supply to actuate the DC contact MEMS switch. The first one is the DC connection to the membrane which connects to the input transmission line ("RF IN" in Figure 31); the second one is to the bottom electrode which connects to a separate DC probe pad, the third one is the DC supply to the bottom metal contact point which connects to the RF output transmission line. Again, we can use two DC bias tees for the DC supply to the RF lines (the input and output RF transmission lines). While the DC supply to the bottom electrode will be

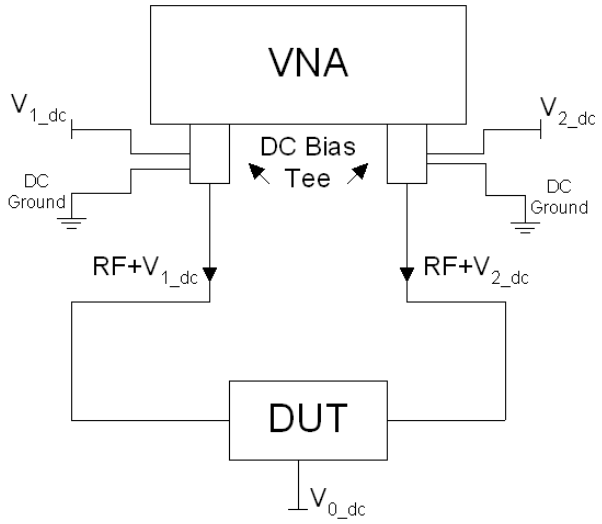



**Figure 33:** Measurement setup schematic for the cantilever DC contact MEMS switches

applied through the DC probe pad. This setup is shown in Figure 33.

As shown in Figure 33, the DC ground can be applied to the DC pins of the bias tees ($V\_1_dc = V\_2_dc = 0$), and delivered to both ports of the MEMS switch along with the RF signals. The actuation voltage ($v\_0_dc$ in Figure 33) is applied to the DC probe pad and then delivered to the bottom electrode of the MEMS switch. The "DUT" in Figure 33 is the DC contact MEMS switch in CPW configuration.

The measurement was done by using an Agilent 8510C VNA, two GGB industries RF probes with a pitch of 150 $\mu$m for the on-wafer probing, and a Cascade DC probe for the DC application.

The s-parameters of the DC contact MEMS switch were taken in order to extract the off-state capacitance and the on-state resistance. The measured results were curve-fitted to the simulated results from the MEMS switch equivalent circuit model in Figure 34 [1].

As it is shown in Figure 34, when the DC contact MEMS switch is at the off- state (the membrane at the up position), it is modeled as a small inductance of 120 pH in series with a small resistance of 0.5 $\Omega$ and a small capacitance of 12 fF, and in parallel connection with a small capacitance of 10 fF. The capacitance of 12 fF is from the parallel plate between the membrane and the bottom contact metal connecting to the output transmission line, while

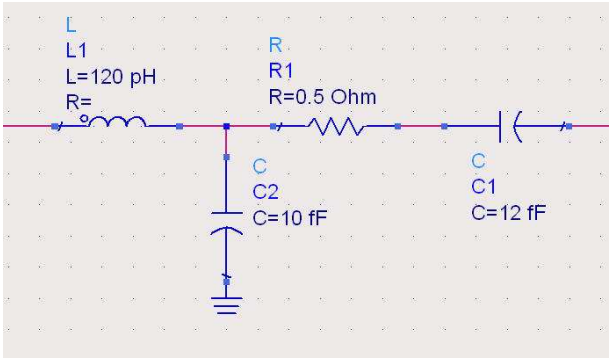



**Figure 34:** Equivalent circuit model of the cantilever DC contact MEMS switch at the off-state

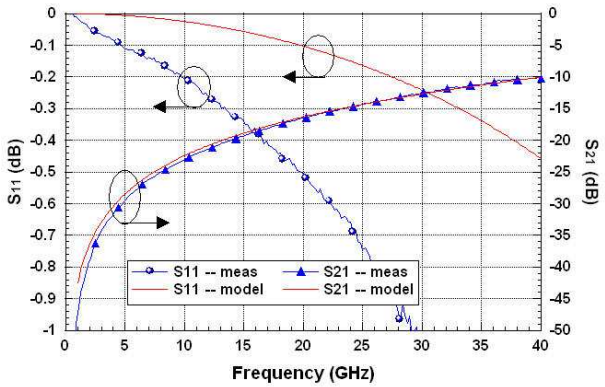



**Figure 35:** Measured vs simulated S-parameters of cantilever DC contact MEMS switch at off-state

the parallel capacitance of 10 fF is from the parallel plate between the membrane and the bottom electrode. The 0.5 Ω resistance is used to model the transmission line loss.

Figure 35 shows that the simulated results from the equivalent circuit model in Figure 34 give a very good agreement with the measured results. As shown in Figure 35, when the DC contact MEMS switch is at the off-state, it has an isolation of about 22 dB at 10 GHz, and a return loss of about 0.2 dB at 10 GHz.

When the actuation voltage is applied between the membrane and the bottom electrode, the switch will be activated and at the on- state (or the membrane will be pulled down and in DC contact with the bottom contact metal in Figure 31), thus, it will exhibit a very small contact resistance which is extracted to be around 0.5 Ω from the simulations. The equivalent circuit model is shown in Figure 36. As it can be seen, when the DC contact MEMS switch is at the on-state, it is modeled as a small inductance (120 pH) in series

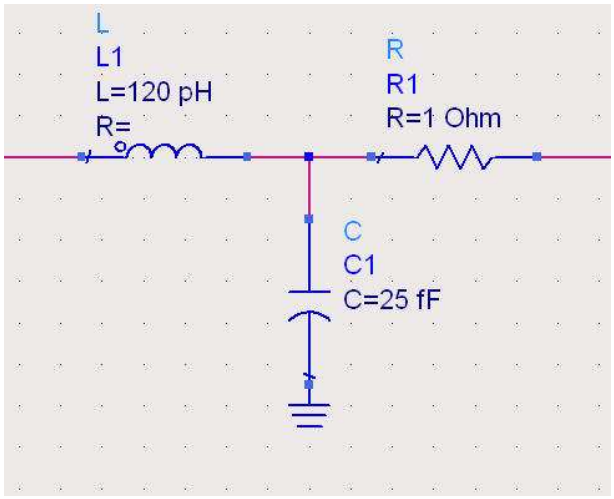



**Figure 36:** Equivalent circuit model of the cantilever DC contact MEMS switch at the on-state

with a small resistance (1 Ω) and in parallel connected with a capacitance of around 25 fF. The inductance of 120 pH keeps the same as when the MEMS switch is at off- state. Since the membrane is in DC contact with the bottom output transmission line at the on-state, the series capacitance is removed, instead it shows a slightly higher resistance compared to the equivalent circuit model at the off- state (Figure 34). This resistance is partially from the small transmission line loss (0.5 Ω in Figure 34), and partially from the MEMS contact resistance. Also noted in Figure 36, the capacitance in parallel is slightly larger than the parallel capacitance in Figure 34 when it's at the off-state. This is because when the MEMS switch is at the on-state, the membrane is pulled closer to the bottom electrode, thus, the capacitance produced by these two overlapped metal plates is larger. This can be found out from the fundamental capacitance formula $C = \frac{\epsilon A}{d}$, where C is the capacitance, $\epsilon$ is the dielectric constant of the vacuum, A is the parallel plate area, and d is the distance between the two parallel plates.

Figure 37 shows that the simulated results from the equivalent circuit model in Figure 36 gives a very good agreement with the measured results. As shown in Figure 37, when the cantilever DC contact MEMS switch is at the on-state, it has an insertion loss about 0.1 dB at 10 GHz, and a return loss about 30 dB at 10 GHz.

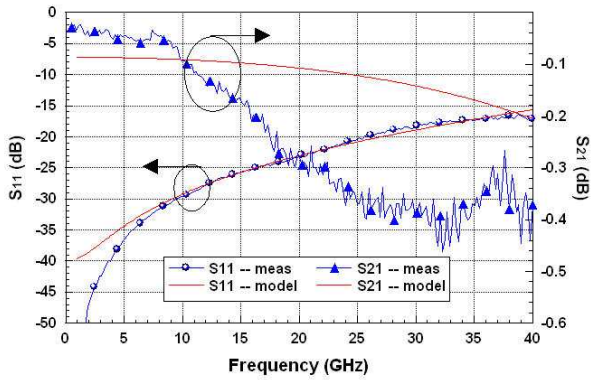



**Figure 37:** Measured vs simulated S-parameters of cantilever DC contact MEMS switch at on-state

## *3.3 Conclusions*

In this chapter, both cantilever capacitive and cantilever DC contact RF MEMS switches have been studied, and their RF performance has been demonstrated. The MEMS switches were fabricated and tested on high resistivity silicon wafers. The equivalent circuit models for both types of the MEMS switches were proposed; the measured results were curve fitted to the simulated results, to extract the off-state capacitance and the on-state capacitance or on-state resistance. The results have shown that both types of the MEMS switches provide an excellent RF performance over a wide band frequency range.

The detailed fabrication process can be found in Appendix II for the capacitive MEMS switches and Appendix IV for the DC contact MEMS switches.

# CHAPTER IV

# X-BAND RECONFIGURABLE BANDSTOP FILTER USING RF MEMES SWITCHES

## *4.1 Motivation*

Very often various communication transceiver systems experience spurious signal interference. When RF/microwave systems are in the receiving mode, not only do they receive the desired signal, but also receive all the spurious signals superimposed to the desired signal, which have to be removed by the frond-end filters to alleviate the load for the back end circuity, as well as maintain a good sensitivity. Among all the interference signals, there is one signal called image frequency interference, which is impossible to get rid of in the back-end of the receiver. Thus, a front-end image rejection filter must be presented immediately after the LNA (Low noise amplifier), and before the back-end circuitry. The image rejection filter should not be in front of the LNA since it will increase the noise figure of receiver systems. More often, a multi-band receiver will need to reject different image frequencies regarding different desired frequencies, thus, a multi-band or tunable image rejection filter is desired for a wireless transceiver.

There are two ways to achieve the multi-band filtering: one is to design multiple image rejection filters for each of the image frequency, and electrically or mechanically choose each filter as desired. The advantage of this method is it is very easy to design, since each filter is only required to resonate at one single frequency. But due to the multiple filters for different signal filtering, it will take a large space and increase the cost, which is not much desired in a compact wireless system since there is always limited space. Instead, the other approach is to have one monolithic tunable bandstop (or notch) filter, which can be used to filter out the spurious signals by using several tuning or switching elements. This will tremendously reduce the circuitry size and lower the cost.

To implement the reconfigurable filter, the circuit topology and the tuning elements have to be chosen. How to achieve the tunability while maintaining the required optimum performance, in terms of miniaturization, low power, low cost, and low loss is the key criteria to consider which technique should be used. There are many different types of transmissions lines available for microwave circuits design and development, such as microstrip lines, CPW (coplanar waveguide), striplines, suspended striplines, and slotted lines, etc. To meet the fabrication limitations and lower the fabrication cost, microstrip lines and CPW lines are the most suitable type of transmissions lines for this design. Both of them have the advantage of ease of fabrication, low cost and low loss. The microstrip transmission line was used because it eases the design process compared to the CPW lines. But as indicated in chapter 2, since most of the RF probes are in CPW configuration, a transition from the microstrip line to CPW RF probe pad has to be designed to facilitate the on-wafer measurements.

Using microstrip transmission lines, a three pole quarter wave length open-circuited bandstop filter [26] was used for the tunable bandstop filter design. The tuning elements of the filter determine the tuning range of the filter as well as the loss. The available tuning devices include PIN diodes, varactors, FET transistor, MEMS switches and MEMS varactors. Due to the superior RF performance of the MEMS devices as shown in Chapter 3, they are chosen as the tuning devices for the reconfigurable bandstop filter. MEMS switches are used in the tunable filter design instead of MEMS varactors due to their higher tuning range.

The tunable bandstop filter will have resonant frequencies at 8, 10, 13, and 15 GHz. By using RF MEMS switches, the goal is to develop a four-state or "2-bit" tunable bandstop filter from 8-15 GHz. More specifically, the filter is designed to have a notch at 8, 10, 13, and 15 GHz, respectively, which can be selected electronically by activating the appropriate MEMS switches. The cantilever beam capacitive MEMS switches with electrostatic actuation were chosen for the filter design based on its advantages as follows: first, comparing with the DC contact MEMS switches, it can typically handle more RF power; second, it's easier to design and fabricate for the microstrip circuits over the air-bridge capacitive switch. For comparison purposes, a set of bandstop filters with the perfect shorts and opens for the

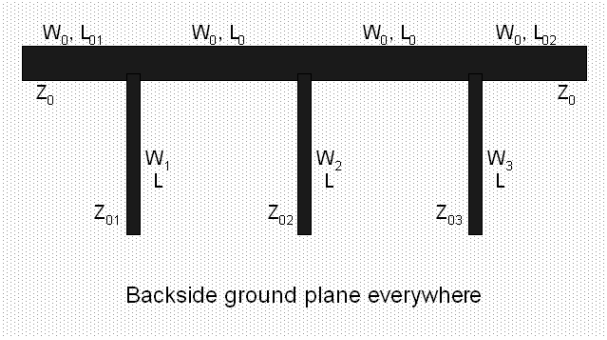



**Figure 38:** The schematic of a bandstop filter using shunt open-circuited microstrip stubs. where, $W_0$ and $L_0$ are the width of the transmission line with characteristic impedance of 50 $\Omega$, and quarter wavelength; $L_{01}$ and $L_{02}$ are the lengths of the feedline at both sides of the filter; $Z_{01}$, $Z_{02}$ and $Z_{03}$ are the characteristic impedance of three shunt stubs; $W_1$, $W_2$ and $W_3$ are the widths of three shunt stubs; L is the length of the three shunt stubs.

ideal model of the MEMS switches, when the membrane is in the down and up positions, was also designed, fabricated and tested.

## *4.2 Reconfigurable Filter Design and DC Bias Lines Implementation*

### 4.2.1 Filter Design

The bandstop filter using quarter-wave length open-circuited resonators is one type of configuration commonly used for filter design [26, 49]. The schematic of this type of filter is shown in Figure 38. As shown in Figure 38, a microstrip line based bandstop filter can be constructed by using a few sections of quarter wavelength ($\lambda_g/4$) transmission lines. In Figure 38, the bandstop filter has three open-circuited microstrip stubs that are quarter wavelength ($\lambda_g/4$) long at the design frequency. Meanwhile, these three quarter wavelength microstrip stubs are separated by two other sections of microstrip lines also that are also quarter wavelength ($\lambda_g/4$) long.

To start the design, the four filters that resonate at 8, 10, 13, and 15 GHz were first designed, as if a group of individual bandstop filters with a single resonant frequency were desired. The characteristic impedances of the microstrip stubs in Figure 38 were calculated at each resonant frequency from Equation (4) [26]:

$$Z_{0n} = \frac{4Z_0}{\pi g_n \Delta} \tag{4}$$

where n = 1, 2, 3, $Z_{0n}$ is the characteristic impedance of each stub; $Z_0$ is the characteristic impedance of the microstrip feed line, which is 50 Ω; $g_n$ is the equal ripple (0.5 dB) low pass prototype value, which can be found in [26,49]; and Δ is the fractional bandwidth.

In order to develop one bandstop filter that can resonate at four different frequencies using RF MEMS switches, these four individual filters need to be combined together. To achieve this, we first need to choose a nominal value of the microstrip line width as the feed line of the tunable filter, since the microstrip line widths are slightly different at different resonant frequencies. To do so, the 50 Ω line width at 10 GHz was chosen, because it is around the center of the full frequency range. The physical dimension for the microstrip feed line can be calculated from the equations given in [26], or simply from the LinCalc function in Agilent ADS. This value was found to be 330 $\mu$m for a 50 Ω characteristic impedance at 10 GHz on a 400 $\mu$m thick high resistivity silicon substrate. For the open-circuited microstrip stubs, their characteristic impedances were calculated and the results are shown in Table 1.

As it is shown in Table 1, the characteristic impedances of the open-circuited microstrip stubs are calculated with respect to both 5% and 10% bandwidths. In order to achieve less than 10% bandwidth, a very high characteristic impedance is required ($Z_{0n} > 398$ Ω), which results in a physical width of the microstrip stub of less than 0.02 $\mu$m. With the standard lithography system available at the Georgia Tech cleanroom, it is impossible to implement, and this feature will dramatically increase the fabrication cost. Another issue with this extremely narrow line is the filter will be very lossy at the passband. In order to make the fabrication easier, reduce the loss and lower the fabrication cost, the physical stubs width was finally chosen as 20 $\mu$m, which corresponds to around 30% bandwidth. A much smaller bandwidth was achieved in the final design by wrapping around the shunt stubs. Extensive Simulations and optimizations were done by using the EM simulator Agilent ADS/momentum to achieve a much smaller bandwidth, with the trade off of the slightly lower band rejection.

**Table 1:** Calculated characteristic impedances of the shunt open-circuited microstrip stubs, for 5% and 10% bandwidth

| N | $g_n$ | $Z_{0n}$ 5% | $Z_{0n}$ 10% |
|---|---|---|---|
| 1 | 1.5963 | 797.6 | 398.8 |
| 2 | 1.0967 | 1160.98 | 580.5 |
| 3 | 1.5963 | 797.6 | 398.8 |

**Table 2:** Calculated physical lengths of the shunt stubs at different frequencies

| Freq (GHz) | 8 | 10 | 13 | 15 |
|---|---|---|---|---|
| Shunt Stub Length ($\mu$m) | 3625 | 2893 | 2218 | 1917 |

$W_1 = W_2 = W_3 = 20$ $\mu$m

After finding the parameters for the 50 Ω microstrip line width and the open-circuited microstrip stubs, we need to find out the physical lengths (with electrical length of $\lambda_g/4$) of those stubs according to different resonant frequencies. This was also done using Agilent ADS LinCalc function. The results are shown in Table 2. The model used in the this function doesn't include the fringing effect of the microstrip transmission line, so the calculated results are slightly different from the Electromagnetic simulation tool (Agilent Momentum), but it can be used as a very good design guide tool to start the design.

So far, all the physical parameters for four different bandstop filters have been obtained. The next step is to compare the physical lengths of the microstrip shunt stubs at each resonant frequency, and replace those fixed stubs with partially fixed microstrip transmission lines connected to the tunable elements. To do so, we need to first find out the difference of the physical lengths for all four resonant frequencies. Since the electrical lengths of the open-circuited shunt stubs all equal to 90°, or quarter wavelength, their physical lengths are different as in Table 2 and Equation (5), where $\lambda_g$ is the guided wavelength, $v_p$ is the phase velocity, c is the light speed, and $\epsilon_{eff}$ is the effective dielectric constant. Equation (5) shows the physical length of the microstrip transmission line is inversely proportional to the resonant frequency. Thus, at the highest design frequency, ie., 15 GHz, the shunt stub

has the shortest physical lengths, which is shown in Table 2.

$$l = \frac{\lambda_g}{4} = \frac{v_p}{4f} = \frac{c}{4f\sqrt{\epsilon_{eff}}} \tag{5}$$

From Table 2, it can be easily seen, that when the frequencies get higher, the physical lengths of the open-circuited microstrip stubs become shorter. Since the tunable elements (MEMS switches) will be used to realize the tunability for the bandstop filter design, the quarter wavelength open-circuited microstrip stub was replaced by a partially fixed microstrip line connected to a lumped element, with the total impedance from these two elements electrically equals to the original quarter wavelength microstrip open-circuited stub, thus, the new filter still resonates at the same four frequencies.

The critical part is to find out the length of the partially fixed microstrip line. To do so, we need to find out the values of the capacitance or inductance that are connected to the fixed transmission line. To find out the value of these lumped elements, we need to know the values of the tunable elements used. Since the capacitive RF MEMS switches presented in Chapter 3 were used in the tunable filter design, when the MEMS switches are at the off-state, their capacitance is around 20 fF; while when they are at the on-state, they exhibit a capacitive RF through path with a high capacitance around 900 fF $\sim$ 1 pF. Equations (6) and (7) show the conversion from a lumped capacitor and inductor to a microstrip line. As in Equation (6), it shows the value of a capacitor increases when the electrical length (thus, the physical length) of the microstrip line increases, when the microstrip line length is less than $\lambda_g/4$; while from Equation (7), it shows the value of an inductor decreases when the electrical length (thus, the physical length) of the microstrip line increases. In this case, the electrical length of the microstrip line exceeds the $\lambda/4$.

With the knowledge of the MEMS switch off-state and on-state capacitances, and by using Equations (6) and (7), we know when a MEMS switch is at the off-state, it has a smaller capacitance and corresponds to a shorter microstrip line; when it's at the on-state, it has a larger capacitance and corresponds to a longer microstrip line. When the physical length exceeds $\frac{\lambda_g}{4}$, it has a positive reactance, thus it is equivalent to an inductor.

This procedure is shown in Figure 39. As shown in Figure 39, the lumped element

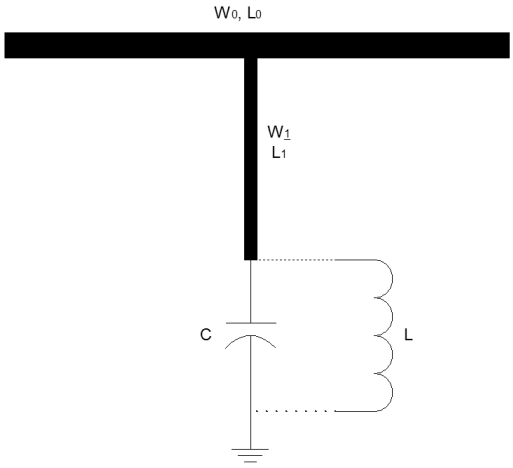



**Figure 39:** Microstrip stub with partially fixed length connected to a lumped element, where $W_0$ and $L_0$ are width and length of the microstrip feedline, $W_1$ and $L_1$ are the stub width and partially fixed stub length.

connected to the partially fixed microstrip line can be either a capacitor (C) or an inductor (L), depending on the required reactance from these lumped elements to produce the same resonant frequencies of the filter. Also noted in Figure 39, only one stub was shown as an example; the conversion of the other two stubs was done in the same manner.

$$\frac{1}{j\omega C} = -Z_{0n}\cot(\beta\ell) \tag{6}$$

$$j\omega \text{Ł} = -Z_{0n}\cot(\beta\ell) \tag{7}$$

To calculate the fixed transmission line length, 10 GHz was chosen as the starting frequency, assuming the filter resonates at this frequency when all the MEMS switches are at the off-state. Since there are a total of four desired resonant frequencies, at least two MEMS switches should be used in parallel for each stub, which will form a 2-bit circuit, and result in a total of four resonant frequencies. This indicates that each stub will finally be split into two sub-circuits. Since the MEMS switch has about 20 fF of an off-state capacitance, when both MEMS switches are at the off-state, the total capacitance C is the sum of two MEMS switch off-state capacitance, which is around 40 fF. By using Equation (6), the actual physical length $\ell_C$ (equivalent to C = 40 fF) can be found. Consequently,

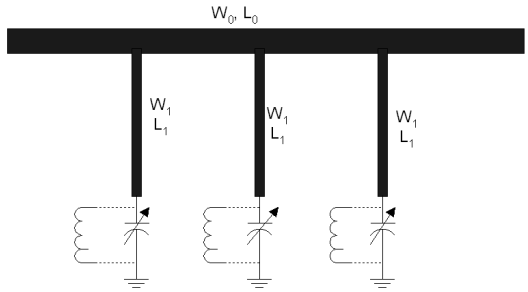



**Figure 40:** Equivalent schematic of the filter with fixed transmission line lengths and tunable capacitors

**Table 3:** The required equivalent capacitances/inductances for different resonant frequencies

| Freq (GHz) | 8 | 10 | 13 | 15 |
|---|---|---|---|---|
| L or C value | 1.12 nH | 40 fF | 264.5 fF | 356 fF |

the fixed length can be found from $\ell_1 = \ell - \ell_C$. $\ell$ is the open-circuited stub length for each resonant frequency. With this value, the varying stub length $\ell_C$ (or $\ell_L$ for the other three frequencies can be calculated, which can be converted to certain capacitance or inductance using equations (6) or (7).

The schematic of the bandstop filter with the above implantation is shown in Figure 40. The schematic shows each stub now has a partially fixed microstrip line connected to the a tunable element (a capacitor or an inductor). The equivalent values of the lumped elements are shown in Table 3.

Table 3 shows that an inductance of 1.12 nH is needed for the filter to resonate at 8 GHz, a 264.5 fF and a 356 fF capacitance are needed for 13 GHz and 15 GHz, respectively, for the schematic shown in Figure 40.

These lumped components were then broken into two sub-circuits connected in parallel. The purpose of this step is to accommodate one MEMS switch in each sub-circuit. This procedure is shown in Figure 41. As shown in Figure 41, the sum of two lumped components in series forms one sub-circuit, which is a two-state variable capacitor ($C_1$ or $C_2$ in series with another fixed lumped component ($C_3$ or $L_4$). The two-state variable capacitors are

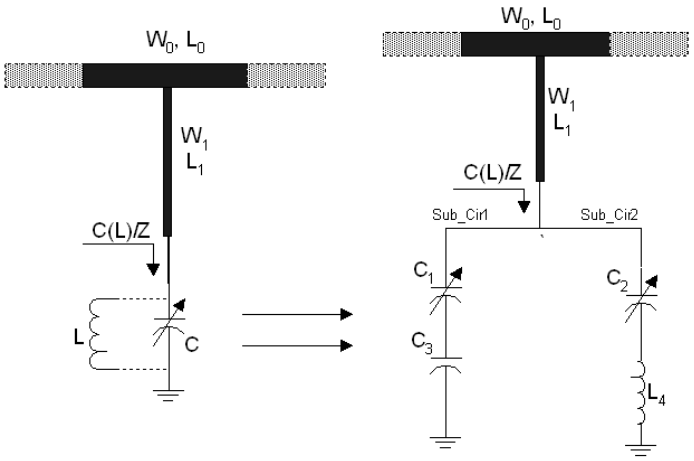



**Figure 41:** Schematic of the capacitor of each path breaking into two sub-circuits

the simplified circuit model of the capacitive MEMS switches, with a value of either 20 fF for the off- state or 900 fF for the on- state.

The values of $C_3$ and $L_4$ can be calculated from Equations (8) to (12), based on the assumption that the sum of the two sub-circuits in Figure 41 produces the same reactance as that of one stub in Figure 40. The initial process of finding the values of $C_3$ and $L_4$ is as follows: 1) when both $C_1$ and $C_2$ are at the off-state, they are both 20 fF. Since they are in series with the other relatively larger capacitance or small inductance, these two capacitors are the dominant components in the series sub-circuit. Thus, the totally equivalent capacitance produced from the sum of the two sub-circuits is around 40 fF; 2) when one of them is at the off-state while the other is at the on-state, eg. $C_1$ is on, while $C_2$ is off, then, $C_3$ will be the dominant one in "sub-cir1", while $C_2$ is still the dominant one in "sub-cir2", thus, the total capacitance is found to be around 356 fF; 3) when $C_1$ is off and $C_2$ is on, the value of $L_4$ will be the dominant one, and the equivalent reactance is produced by this inductance; 4) when both $C_1$ and $C_2$ are on, each of them has a value of 900 fF, which is a relatively large capacitance, thus, the other components connected to them will be the dominant ones. The equivalent capacitance will be calculated as if just $C_3$ and $L_4$ are in parallel connection, with a value of 264.5 fF. Thus, by choosing $C_1$ and $C_2$ at different states (or MEMS switches at on or off), the different resonant frequencies will be selected. The following equations are used for the filter design:

$$Z = \frac{Z_1' Z_2'}{Z_1' + Z_2'} \tag{8}$$

$$Z_C = \frac{1}{j\omega(C)} \tag{9}$$

$$Z_L = j\omega \text{Ł} \tag{10}$$

$$Z_1' = \frac{1}{j\omega(C_1)} + \frac{1}{j\omega(C_3)} \tag{11}$$

$$Z_2' = \frac{1}{j\omega(C_2)} + j\omega \text{Ł}_4 \tag{12}$$

Where Z is the total impedance (reactance) corresponding to the total capacitance C or inductance L and $\omega$ is the angular frequency. $C_1$ and $C_2$ are two-state variable capacitors which are used as the MEMS switch circuit model on- and off-state capacitance values.

The results are summarized in Table 4, which shows the equivalent lumped component values required for the tunable bandstop filter with the resonant frequencies at 8, 10, 13, and 15 GHz.

After combining the fixed microstrip transmission lines with the lumped elements together, a tunable bandstop filter with partially fixed transmission lines and the lumped elements has been designed. The schematic is shown in Figure 42.

As it can be seen from figure 42, the tunable bandstop filter has three stubs, and each stub consists of a partially fixed transmission line connected to two sub-circuits in parallel connection. Equivalently, each stub will produce the same electrical length as that of the original individual filter, which enables the tunable filter to resonate at the same frequencies.

The equivalent components' value for $C_3$ and $L_4$ needed for the combined tunable bandstop filter is shown in Table 5.

**Table 4:** The equivalent capacitance or inductance produced from the sum of the two sub-circuits with respect to different states of $C_1$ and $C_1$, as well as the resonant frequencies

| $C_1$ | $C_2$ | equivalent reactance | equivalent components' value | frequency (GHz) |
|---|---|---|---|---|
| off (20 fF) | off (20 fF) | Z $\cong Z_{C_1} + Z_{C_2}$ | 40 fF | 10 |
| off (20 fF) | on (900 fF) | Z $\cong Z_{L_4}$ | 1.12 nH | 8 |
| on (900 fF) | off (20 fF) | Z $\cong Z_{C_3}$ | 356 nH | 15 |
| on (900 fF) | on (900 fF) | Z $\cong Z_{L_4} + Z_{C_3}$ | 264.5 nH | 13 |

where, Z is the total equivalent impedance or reactance seen at the sum of the two sub-circuits; $Z_{C_1}$, $Z_{C_2}$, $Z_{C_3}$, and $Z_{L_4}$ are the equivalent impedances or reactances from $C_1$, $C_2$, $C_3$, and $L_4$.

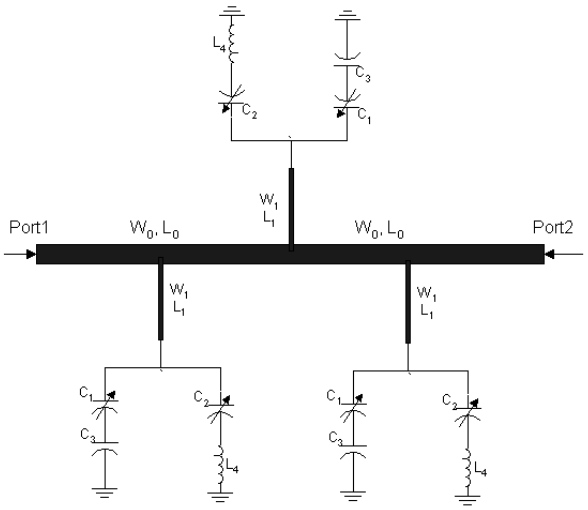



**Figure 42:** Schematic of the tunable bandstop filter with fixed distributed transmission line and lumped elements

**Table 5:** The equivalent capacitances and inductances for two sub-circuits

| $C_1$ (fF) | $C_2$ (fF) | $C_3$ (fF) | $L_4$ (nH) |
|---|---|---|---|
| 20/900 | 20/900 | 356 | 1.12 |

**Table 6:** The correspondent resonant frequencies with respect to the different combinations of $C_1$ and $C_2$

| $C_1/C_2$ (fF) | Resonant Frequency (GHz) |
|---|---|
| 20/20 (off/off) | 10 |
| 20/900 (off/on) | 8 |
| 900/20 (on/off) | 15 |
| 900/900 (on/on) | 13 |

The tunable filter with lumped elements has now been designed, and the resonant frequency is determined by selecting the different combinations of capacitors $C_1$ and $C_2$, which is shown in Table 6.

The simulations and optimizations for the tunable bandstop filter with partially fixed transmission lines and the fixed lumped components were done using Agilent ADS. The optimizer used was the gradient method to get the right resonant frequencies and the optimum bandwidth ($< 10\%$).

In order to design a monolithic microstrip line based tunable bandstop filter, the fixed lumped components were replaced with the microstrip transmission lines with the fixed physical length ending with radial stubs that give the desired reactance. EM simulations by using Agilent Momentum (with Method of Moment) were performed, to make sure that the radial stubs chosen have the same reactance with the lumped elements they are replacing. Meanwhile, the digital variable capacitors $C_1$ and $C_2$ were replaced with the perfect shorts and opens for the ideal model of the MEMS switches, when they at the on- and off-state, respectively.

The tunable bandstop filter performance was simulated and fine tuned with the full-wave EM simulation tools: the Ansoft HFSS and Agilent momentum. Figure 43 shows the magnitude of the E-field distribution at 10 GHz from the HFSS simulation, which is used as a demonstration of how this bandstop filter works. As it is shown in the figure, most of the energy is blocked and concentrated at the first two stubs with very little energy leaking out to the second port through the 50 $\Omega$ feedline.

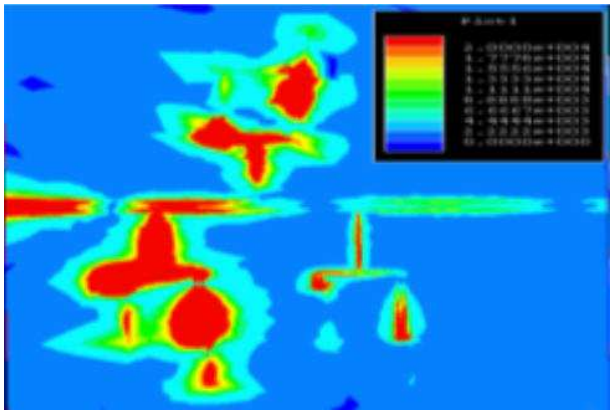


**Figure 43:** The E-field distribution (magnitude) from HFSS simulation at 10 GHz

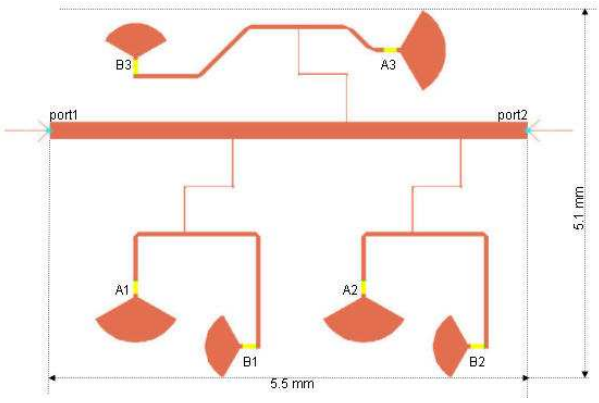



**Figure 44:** Microstrip tunable bandstop filter layout with MEMS switches models

After the desired performance was acquired with this approach, the real MEMS switches model in Agilent Momentum was placed at the location of the perfect open and short. More extensive simulations and optimizations were done to achieve the desired tunable bandstop filter response, in terms of both the rejection and bandwidth. The layout is shown in Figure 44.

Figure 44 shows that there are a total of six MEMS switches used in the tunable filter design, with one in each sub-circuit of the microstrip stubs. The MEMS switches are divided into two groups, which are noted as An and Bn (with n = 1, 2, 3) in Figure 44. All the MEMS switches of An will be operated at the same state, while all Bn will be at the same state. The operation modes will give a total of four different combinations, which correspond to the four different resonant frequencies. The tunable filter size is 5.5 mm x 5.1 mm, and the RF energy is excited through port1.

To facilitate the on-wafer measurements, the CPW RF probe pad to microstrip transition developed previously needs to be added to both sides of the microstrip feeding lines.

### 4.2.2 DC Bias Lines Implementation

In order to appropriately actuate the MEMS switches, the DC bias lines have to be carefully designed and implemented. The purpose of having the DC bias lines is to provide the DC voltage between the MEMS switches membrane and the bottom electrode, as well as to prevent the RF energy leakage through the DC bias lines.

As it is shown in the cross section of the capacitive MEMS switches shown in Figure 23 in Chapter 3, there are two DC bias lines needed to be connected for the MEMS switch actuation: the first one is for the connection to the membrane, or the "input" transmission line of the MEMS switches; and the second one is for the connection to the bottom electrode, or the "output" transmission line of the MEMS switches. As it is shown in Figure 44, all the MEMS switches in the tunable bandstop filter have one common connection through the 50 $\Omega$ transmission line at one side of the MEMS switches, which connects to the membranes of all the MEMS switches. However, the other side of the MEMS switches are connected to the individual radial stubs, which are separate from one another.

Thus, for one side of the MEMS switches that has the common connection, a common DC ground can be provided through the RF line. This can be done in the following procedure: 1) connect a DC bias Tee between the VNA (vector network analyzer) and the tunable filter (DUT), 2) apply the DC ground to the DC bias Tee, thus, at the output of the DC bias Tee, both RF signal and DC ground will be applied to the center pin of the RF probe, which will be connected to the 50 $\Omega$ RF line at the time of on-wafer probing. Meanwhile, for the other side of the MEMS switches, the positive voltage need to be provided to each individual radial stubs. The DC probes can not be applied immediately onto the radial stubs, since this will load the circuit and alter the filter response. Thus, the DC bias lines are needed for this purpose.

For the tunable bandstop filter, the DC bias line is made of a very narrow line (10 $\mu$m) metallized with electro-plated gold. An appropriate length was chosen to achieve a very


**Figure 45:** Layout of the DC bias line for MEMS switch in tunable bandstop filter

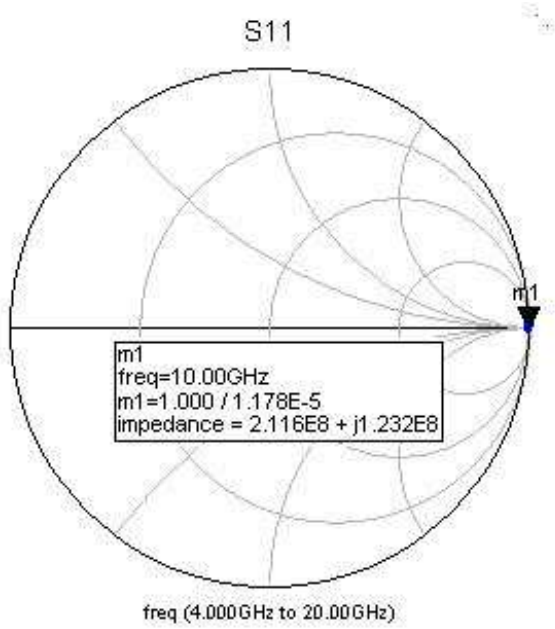



**Figure 46:** Simulated impedances of the DC bias line

high impedance seen at the port connecting to the radial stubs, in order to minimize the loading effects to the filter. Figure 45 shows the layout for a DC bias line, while the response of the DC bias line from the simulation is shown in Figure 46.

In Figure 45, the DC bias line has a width of 10 $\mu$m, and a length of 1 mm. At one end of the line, it has a square pad with a size of 150 $\mu$m x 150 $\mu$m, which is designed as the DC probe pad. The other end (narrow end) or "port1" of the line will be connected to a radial stub. The expected impedance seen at this port is a perfect open.

Figure 46 shows the simulated impedance of the DC bias line at port1. As it is shown with the marker "m1", it has an impedance of $2.1 \times 10^8 + \text{j}1.2 \times 10^8\ \Omega$, which is a perfect open. But when the measurement is being taken, the DC probes will be pulled down onto the DC probe pads (the square pad), which will change the impedance of the DC probe

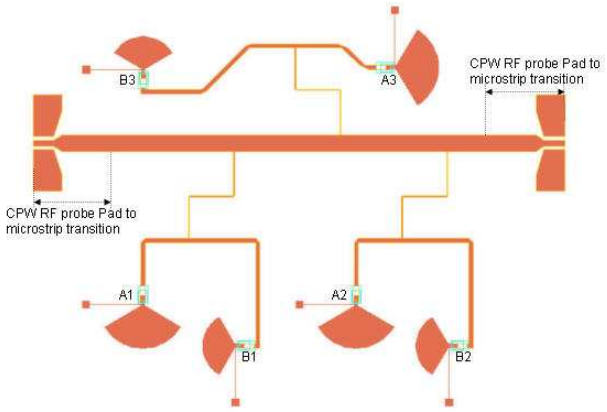



**Figure 47:** Final layout of the tunable bandstop filter with CPW RF probe pad to microstrip transitions and DC bias lines

pad, and consequently, the impedance seen at the port1 will change too. Thus, the DC bias line won't be perfect open any more, and some loading effects will occur. This effect will be shown in the final measured results.

### 4.2.3 Reconfigurable Filter Final Layout

With the completion of the CPW RF probe pad to microstrip transition and the DC bias lines implementation, the tunable bandstop filter reaches its final layout. Figure 47 shows the complete layout of the tunable bandstop filter in the Agilent Momentum simulation. It includes the CPW RF probe pad to microstrip and the microstrip to CPW RF probe pad transitions at both ends of the microstrip line [32]. The transition will be deembeded after the TRL (Through-Reflection-Line) calibration. The measurement reference plane is at both ends of the transition at the microstrip line section.

For the on-wafer measurement purpose, a set of TRL (Through-Reflection-Line) lines were also designed and fabricated on the same wafer with the tunable bandstop filter.

This design process is described for a reconfigurable bandstop filter that has a total of four resonant frequencies, with "2-bit" MEMS switches acting as the digital capacitors. The same topology can be used to expand the design to have more resonant frequencies by adding some more sub-circuits into the microstrip stubs. For example, by adding one more sub-circuit in each of the microstrip stub, there will be a total of three MEMS switches in each stub connected to the radial stubs, which will create a "3-bit" filter, and consequently

result in $2^3 = 8$ resonant frequencies.

## *4.3 Reconfigurable Filter Fabrication*

### 4.3.1 Fabrication Process Flow Development and Layout Generation

The fabrication process flow development and layout generation are two critical steps toward a successful fabrication and a final working device. The layout generation for the tunable filter was done with the Agilent ADS layout function, since all the simulations/optimizations were done with the Agilent Momentum. The layout has been carefully designed so that the maximum number of filters can be fabricated on the same quarter piece of a 4" wafer, in case of yield issues as well as for repeatability testing purposes. In addition, the discrete capacitive MEMS switches were also fabricated on the same wafer to obtain the s-parameters of the MEMS switches. A set of TRL (Through-Reflection-Line) calibration lines were also fabricated on the same wafer for on-wafer measurements, as shown in the upper right corner in Figure 48. The distance between each circuit was carefully measured to be 2 mm which is greater than 5 times of the substrate thickness (400 $\mu$m), in order to minimize the coupling effects or cross talk between the different circuits. The mask file was then generated and sent to the Advanced Reproduction, Inc. (a masking making company) for the final mask making. The final masks are on a set of 4"x4" plates, with the base of soda lime coated with Chromium. The masks totally have 4 layers or 4 different mask plates to complete the fabrication process. The final layout is shown in Figure 48.

As discussed in the previous section, two different types of filters were fabricated: one was the four filters with different combinations of the perfect shorts and opens for the ideal model of the MEMS switches, and the other was the monolithic bandstop filter with the MEMS switches. In both cases, the circuits were fabricated on a high resistivity silicon wafer with $\epsilon_r = 11.7$, $\rho > 20{,}000\ \Omega$ -cm and a thickness of 400 $\mu$m. The backside metallization layer was 3 $\mu$m thick of electro-plated gold.

The first fabricated circuits contain four single-layered microstrip filters, with each of them having one combination of the short and open as the ideal model for the MEMS switch. The second fabricated circuit was a multi-layered tunable bandstop filter using the

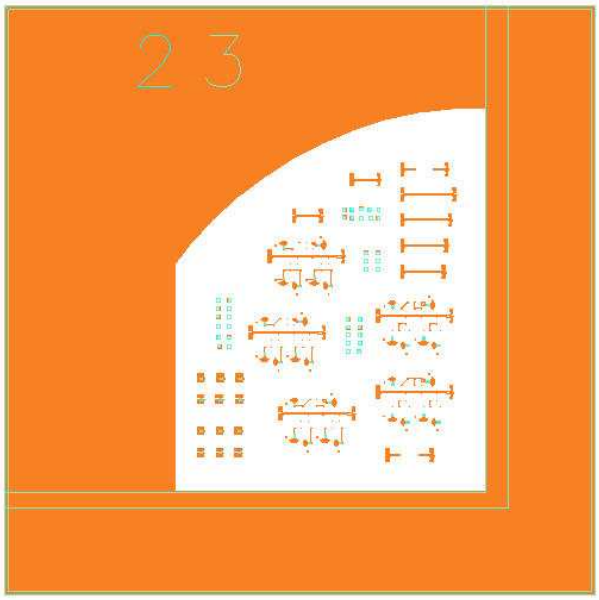



**Figure 48:** Tunable bandstop filter mask layout for tunable filter with MEMS switches

MEMS switches, which is monolithically built on the silicon substrate with the rest of the circuit. In this case, the fabrication steps were as follows: 1) the bottom electrode layer was deposited using the electron-beam evaporator and then patterned; 2) a thin film of silicon nitride ($Si_3N_4$) was deposited (2000 $\mathring{A}$) using the PECVD technique and then patterned to provide the dielectric layer between the bottom electrode and the top membrane; 3) the sacrificial layer using Shipley SC1813 photoresist was spun and then patterned; 4) the top membrane was deposited for the seed layer and then electro-plated to a thickness of 2.5 $\mu$m; 5) the membrane was released by removing the sacrificial layer with photoresist striper; and 6) the critical point dryer was used to dry the circuit to prevent stiction problems during the switch release.

Figure 49 shows the process flow for the reconfigurable tunable bandstop filter. The detailed fabrication process can be found in Appendix II.

The correlation between the different combinations of the perfect shorts and opens, and the different combinations with the MEMS switches is shown in Table 7. The numbering convention is used as "AnBn" for each combination. For example, when the switches of An-Bn has the combination of "on-off", the filter response will be corresponding a perfect

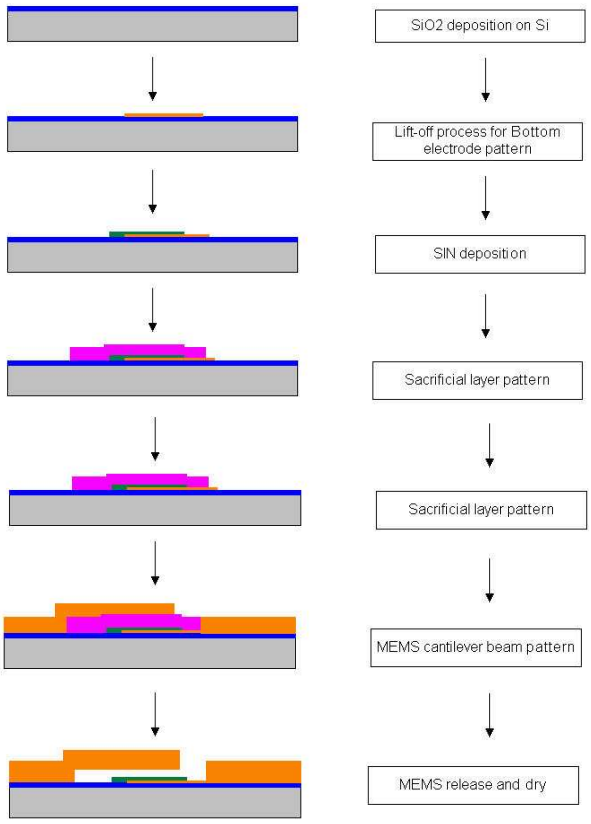



**Figure 49:** Fabrication process flow for tunable bandstop filter with cantilever capacitive RF MEMS switches

**Table 7:** The correlation between the MEMS states and the perfect short/open with respect to the different resonant frequencies

| Resonant Frequency (GHz) | 8 | 10 | 13 | 15 |
|---|---|---|---|---|
| Perfect open/short | open-short | open-open | short-short | short-open |
| MEMS Switches | off-on | off-off | on-on | on-off |

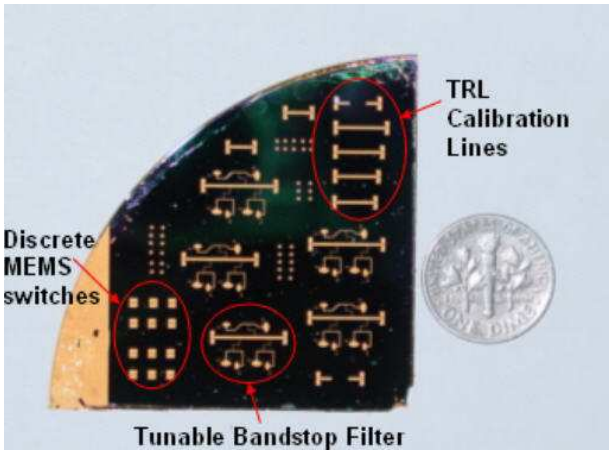



**Figure 50:** Fabricated circuits of the tunable filter with MEMS switches

short/open filter with a "short-open" combination.

Figure 50 shows the picture of the fabricated circuits on a quarter piece of a 4" high resistivity silicon wafer. As shown in Figure 50, the MEMS switches were fabricated separately in order to characterize their electrical performance. The MEMS switches with the same dimensions were used in the tunable filter fabrication. The TRL calibration lines were also included for the de-embedding during the on-wafer calibration and measurement.

Figure 51 is the partial picture of the fabricated circuit taken with the Hitachi 3500H SEM (Scanning Electron Microscope). It shows the CPW RF probe pad to microstrip transition and one switch with the DC bias line.

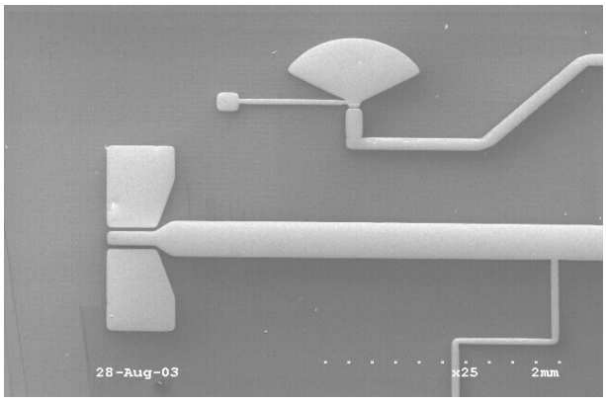



**Figure 51:** SEM picture of the partial fabricated circuit

### 4.3.2 Fabrication Challenges

A lot of complicated problems and challenges have been encountered during the fabrication process. The first one is the silicon nitride ($Si_3N_4$) deposition; a low stress deposition process has been developed in order not to deform the bottom electrode layer underneath the $Si_3N_4$. The quality and thickness of the $Si_3N_4$ can be very critical for the proper operation of the MEMS switches. A $Si_3N_4$ layer with poor quality, such as pores in the material, will lead to a poor isolation between the membrane and the bottom electrode, which will possibly lead to a lower break down voltage of MEMS switches and a higher leakage of the capacitor; the circuits also might be damaged due to some very strong chemical attack, such as Hydrofloride acid (HF), in the later fabrication steps. Thus, a good quality and enough thickness of the $Si_3N_4$ layer must be deposited to protect the bottom electrode. Meanwhile, the thickness of the $Si_3N_4$ can not be too high (typical the thickness is around 2000 $\mathring{A} \sim$ 3000 $\mathring{A}$), otherwise it will cause a dielectric charging problem.

Another issue is the sacrificial layer patterning. A sacrificial layer was patterned prior to the patterning and metallization of the membrane (suspension cantilever beam). This layer will be removed after the membrane formation. Most commonly used material for the sacrificial layer is photoresist. A Shipley SC1813 photoresist was used for this purpose $Si_3N_4$ce it is an inherently thin resist but can still be patterned to 2 $\mu$m thick, by carefully choosing the resist spinning speed and time. Shipley SC1827 is not recommended to use since it's a relatively thicker resist and might not be easy to release in the final membrane

releasing process. One common issue for the sacrificial layer is the seed layer deposition for the membrane, with either an electron-beam (E-beam) evaporator or DC sputter technique. The E-beam evaporator has been used throughout the process due to it's much smoother metal surface, which is extremely important for the cantilever beam MEMS switch. The deposition speed of the seed layer, which is Titanium, Gold and Titanium in sequence, as well as the chamber temperature (low) and vacuum (high) must be carefully considered, in order to acquire the smoothest possible surface while not to crush the sacrificial layer under the seed layer. After the sacrificial layer is covered by the membrane seed layer, all the fabrication process will need to avoid using any photo resist removal solvent, and wafer baking temperatures should be below 80°C. Otherwise the sacrificial layer will be destroyed, thus, lead to fabrication failure.

Gold plating was used for the circuit metallization. For a single-layered circuit fabrication, it is not critical because the purpose is only to cover the substrate with the desired thickness of gold. But for the MEMS Switches or the circuit monolithically fabricated with the MEMS switches, this could become a problem. Thus, the gold plating process has to be well controlled to get good RF MEMS switches. A slow plating process is needed for the membrane to produce a low stress metal layer. If the membrane is plated too fast, it will be greatly deformed. As a result, a very high voltage is need to actuate the switches; or in the worst case, the MEMS switches might not be able to be actuated due to the membrane deformation. On the other hand, the plating process can't be too slow or too long, otherwise, the patterned photo resist will start cracking in the gold plating solution. A very toxic plating solution was used (Cyanide compound) for this purpose. The solution temperature needs to be well controlled at 55°C, and a very stable constant DC current source is needed to provide a 7.5 mA DC current, for gold plating of the circuits on a quarter of a 4" wafer, resulting in $2 \sim 2.5$ $\mu$m thick of gold in 30 min. This gives about 30-35 volts actuation voltage for the MEMS switches.

Last, but not the least is the drying process for the circuits using the MEMS switches. A super critical point dryer provided by Tousimis was used at the last step after the membrane releasing. This step is very important and critical to minimize the stiction problem.

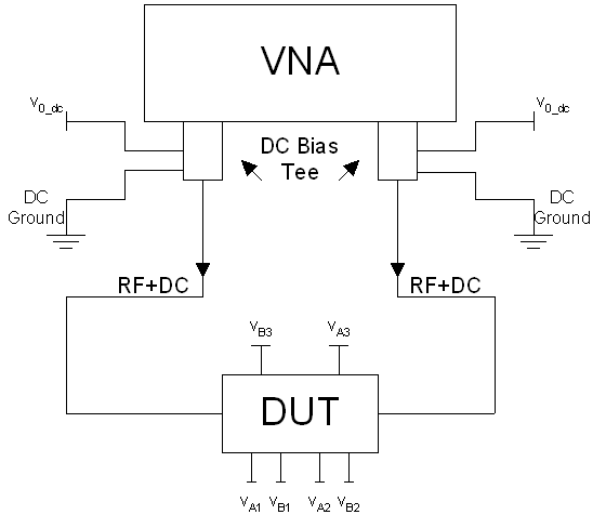



**Figure 52:** Measurement setup diagram for the tunable bandstop filter

## *4.4 Filter Measurements and Results*

The s-parameters measurement for the tunable bandstop filter and the MEMS switches were done by using an Agilent 8510C vector network analyzer and a Cascade probe station. The GGB Industries RF probes with a 200 $\mu$m pitch were used for the RF measurements; while Cascade Microtech probes were used for the DC application to the MEMS switches. The DC ground was provided through the RF path, by using two PicoSecond DC bias Tees. The measured actuation voltage of the cantilever MEMS switches was 30 - 35 volts.

A multi-line TRL (Thru-Reflect-line) calibration technique was used to de-embed the CPW RF probe pad to microstrip transition, and move the reference planes to the locations shown in Figure 47. The program Multical of NIST was used for this purpose [37].

The diagram of the measurement setup is shown in Figure 52.

As it is shown in Figure 52, two DC bias tees were connected to the VNA (vector network analyzer) at one side, and the other side is connected to the DUT (device under test) through the RF cables. The DUT here is for the tunable bandstop filters. Also shown in Figure 52, the DC ground was applied to the DC input pin of the bias tees ($v_{0_{dc}} = 0$). With the RF signal generated from the VNA, the output of the bias tee has two signals: the DC ground and the RF signal, and both of them will be applied to the tunable filter main RF line. The voltages $v_{An}$ and $v_{Bn}$ (n = 1, 2, 3) are the actuation voltages for six

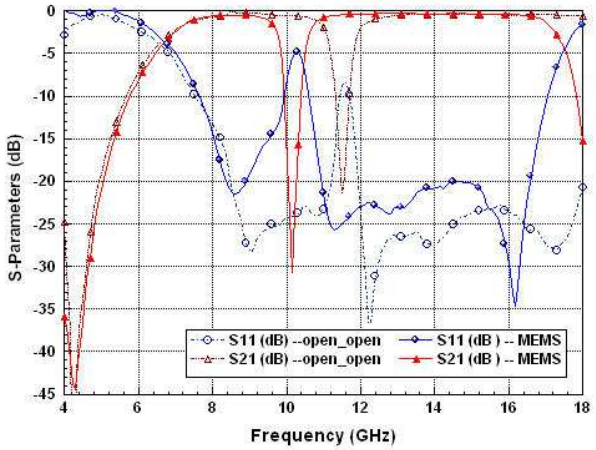



**Figure 53:** Measured results comparison between the circuit with open-open case without MEMS switches and the off-off case with the MEMS switches.

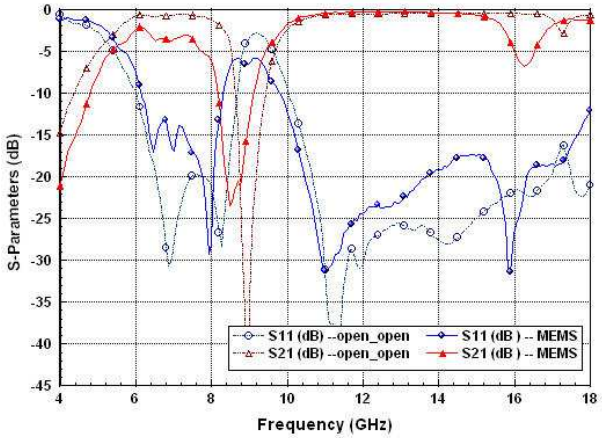



**Figure 54:** Measured results comparison between the circuit with open-short case without MEMS switches and the off-on case with the MEMS switches.

different MEMS switches in the filter, whereby, all An will be operated in the same mode, and all Bn will be operated in the same mode.

The measurements for both cases (four filters with the perfect opens/shorts and with the MEMS switches) were taken. Figures 53 - 56 show the measured s-parameter comparison between the four individual filters with the perfect shorts/opens and the tunable filter with the MEMS switches. One obvious observation is that for all the combinations except the short-short /on-on combination, the resonant frequency shifts and the bandwidth also changes. In all the figures presented below, all the combination sequence follows the order of "AnBn" as in Figure 44, with n = 1, 2, 3.

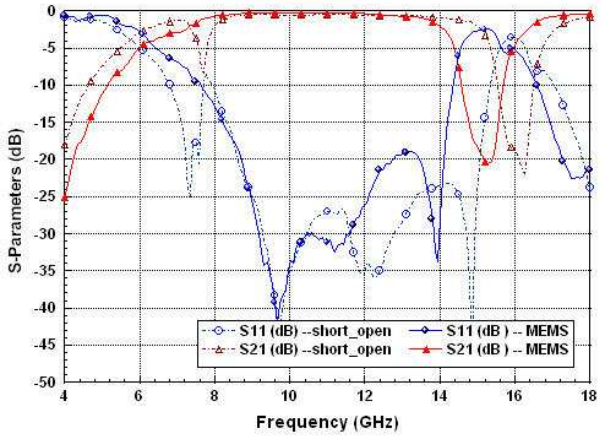



**Figure 55:** Measured results comparison between the circuit with short-open case without MEMS switches and the on-off case with the MEMS switches.

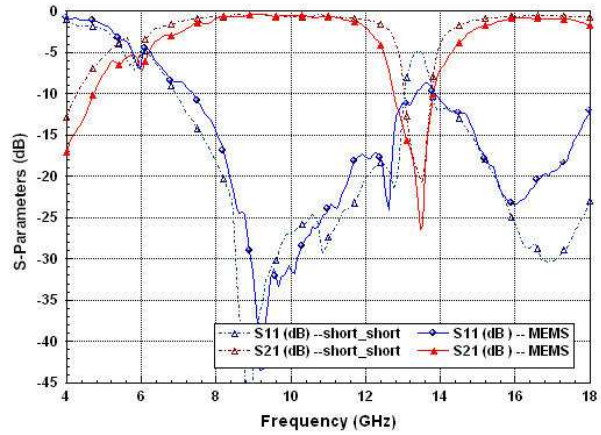



**Figure 56:** Measured results comparison between the circuit with short-short case without MEMS switches and the on-on case with the MEMS switches.

Figure 53 shows the comparison of the measured filter response with the combination of the perfect open-open case and the measured tunable filter response with the off-off state. As it can be seen in Figure 53, the resonant frequency from the first case is around 11.5 GHz, while the resonant frequency from the MEMS filter is at 10 GHz, the frequency has a shift about 1.5 GHz. This big difference is caused by the fact that the MEMS switch at the off-state is a limited capacitance rather than a perfect open circuit. Therefore, due to this capacitive effect from all six MEMS switches, a different resonant frequency for the tunable bandstop filter occurred. However, the response with the MEMS switches is the desired one.

Figures 54 and 55 show the comparison of the measured filter responses with the combination of the perfect open-short, short-open, and the measured tunable filter responses with the off-on, on-off states, respectively. These two figures show that there is still a frequency shift, but the for the first combination with the resonant frequency around 8 GHz, the difference is about 500 MHz; and for the second combination with the resonant frequency around 15 GHz, the difference is about 800 MHz. Compared to the open-open or off-off case, the percentage of the resonant frequency shift is much smaller. This is because in the individual filters, three out of six MEMS switches were modeled as the perfect short, and the other three were modeled as the perfect open. This shows that the perfect short is a better method to model the MEMS switches when they are at the on- state. This also proves in another way, when the MEMS switches are actuated (on-state), the RF MEMS switches provide a good capacitive short to the RF path.

Figure 56 effectively demonstrates that the above analysis is true. In Figure 56, it shows the measured filter response comparison between the individual filter with a perfect short-short combination, and the measured tunable filter response with the on-on state. The resonant frequency for both cases is the same; the only difference is that the bandwidth of the measured tunable filter with that of the MEMS switches is wider than that of the individual filter with the perfect short-short case. This discrepancy is caused by the loading effects from the DC bias lines. Compared with Figure 53, in which both filters have the same bandwidth despite the difference in the resonant frequency. Figures 54 and 55 show

the slight differences of the bandwidth. But when all the MEMS switches are actuated, all the DC bias line contribute loss to the filter, thus, the difference of the bandwidth between these two cases becomes obvious.

A summary of the measured results and a comparison of the measured filter response between four individual filters with the perfect opens/shorts and the measured tunable filter response with the MEMS switches is shown in Table 8. To summarize it, the individual filters with the perfect open/short model shows the resonant frequencies at 9, 11.5, 13.4, and 16 GHz with a measured rejection of -40, -23, -20, and -22 dB, respectively. The percentage bandwidth for the filter at each resonant frequency is 7.8%, 3%, 5.4%, and 5.6%, respectively. For the tunable filter responses with the MEMS switches, the measured rejection at the notch frequencies was -23, -27, -21, and -20 dB and the -10 dB bandwidth was 9.7%, 6.5%, 7%, and 5% for 8, 10, 13 and 15 GHz, respectively. The insertion loss at the passband was measured to be around 0.5 dB, for both cases.

The measured tunable bandstop filter response with the MEMS switches were also compared with the simulated results (Figures 57 to 60), where the MEMS switches were modeled as 28 fF at the off-state, and 1000 fF at the on-state. The off- capacitance and the on- capacitance used here are slightly different from the value extracted from the equivalent circuit model of the capacitive MEMS switches in Figures 27 and 29. This is caused by the variations in the fabrication process.

The simulations were done in two main steps: 1) the tunable bandstop filter EM simulations were done in the Agilent Momentum with the method of moments. Then, in order to have a better comparison between the simulations and the measurements, the MEMS switches were removed and six pairs of the internal ports were inserted into the gaps, where the MEMS switches are located; 2) the simulated results from the Momentum were exported into the Agilent ADS schematic window, and the six capacitors with the variable values were then connected between these six different pairs of the internal ports. These six variable capacitors are used to model the two state MEMS capacitors, which have the value of 28 fF for the off- state, and 1000 fF for the on- state. As shown in Figures 57 to

**Table 8:** Center frequency and bandwidth comparison between the measurement with MEMS switches and perfect open-/short circuits

| | | with MEMS switches | Perfect open/short |
|---|---|---|---|
| off-off/ open-open | Center Freq/Rejection (GHz/dB) | 10.16/-27 | 11.5/-23 |
| | Bandwidth (GHz)* | 0.42 | 0.34 |
| | Percentage BW (%) | 5 | 3 |
| off-on/ open-short | Center Freq/Rejection (GHz/dB) | 8.6/-23 | 9/-40 |
| | Bandwidth (GHz)* | 0.84 | 0.7 |
| | Percentage BW (%) | 9.7 | 7.8 |
| on-off/ short-open | Center Freq/Rejection (GHz/dB) | 15.13/-21 | 16.02/-22 |
| | Bandwidth (GHz)* | 0.97 | 0.89 |
| | Percentage BW (%) | 6.5 | 5.6 |
| on-on/ short-short | Center Freq/Rejection (GHz/dB) | 13.275/-20 | 13.42/-20 |
| | Bandwidth (GHz)* | 1.05 | 0.72 |
| | Percentage BW (%) | 7 | 5.4 |

*The bandwidth was calculated as -10 dB bandwidth.

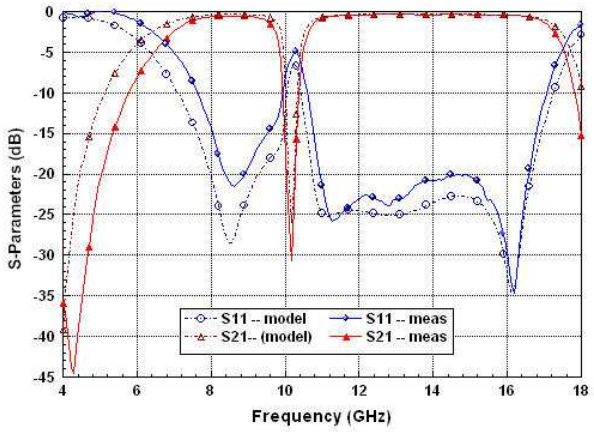



**Figure 57:** Measured and simulated results at 10 GHz with the off-off state of the MEMS switches resonant at 10 GHz.

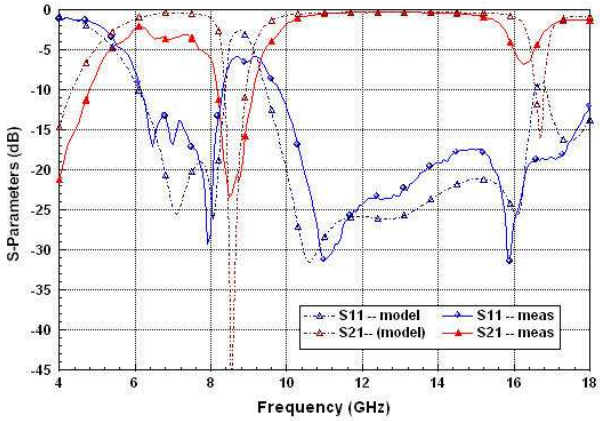



**Figure 58:** Measured and simulated results at 8 GHz with the off-on state of the MEMS switches resonant at 8 GHz.

60, the measurements and the simulations are in a good agreement.

Figure 57 shows the tunable bandstop filter response comparison between the measured and simulated results at the off- state. As it can be seen from this figure, they have an excellent agreement. The resonant frequency is at 10.1 GHz for both cases, the passband insertion loss is about 0.5 dB, and the bandwidth is the same for both cases. This perfect match shows two important aspects of the tunable bandstop filter development: 1) the physical dimensions in the simulations well match that of the real MEMS switch from fabrication; 2)when all the MEMS switches at the off- state, and the DC probes tips were not pulled down onto the DC probe pads which are connected to the DC bias lines, the tunable filter doesn't experience any external loading effects.

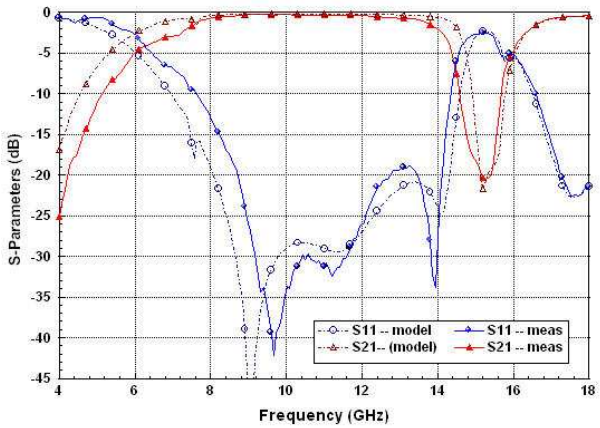



**Figure 59:** Measured and simulated results at 15 GHz with the on-off state of the MEMS switches resonant at 15 GHz.

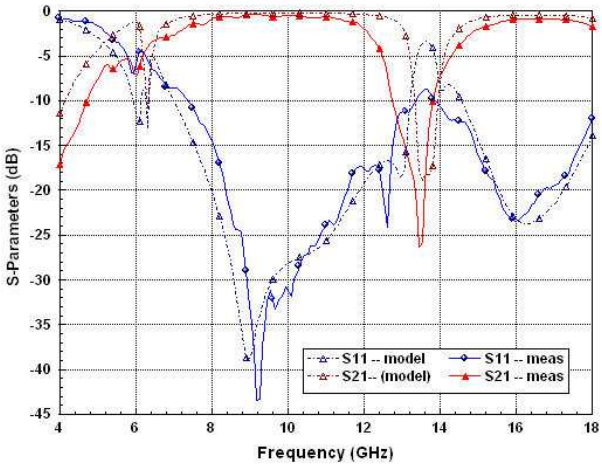



**Figure 60:** Measured and simulated results at 13 GHz with the on-on state of the MEMS switches resonant at 13 GHz.

Figures 58 and 59 show the tunable filter responses comparison between the simulated and the measured results, when the MEMS switches are at the off-on and on-off combinations, respectively. With these two cases, the tunable bandstop filter resonates at 8 GHz and 15 GHz, respectively. They both show some discrepancies in terms of the bandwidth, regardless of the same resonant frequencies. Similar to the analysis above, this is because three out of six MEMS switches were actuated at the same time, and due to the imperfection of the DC bias lines, they are loading the circuit and result in a small RF energy leakage through those DC bias lines.

Figure 60 shows the filter response comparison between the simulation and the measurement when all the MEMS switches are actuated, or at the on-state. It is very obvious in this figure that the measured filter has a much wider bandwidth than the simulated one. This is because when all the MEMS switches are at the on-state, they are actuated through the DC bias lines, and there is significant amount of RF energy leakage through the DC bias lines.

Thus, a good DC bias line is very important for a tunable circuit using the MEMS switches. The improved DC bias lines will be discussed in Chapters 5 and 6.

Figure 61 shows the composite insertion loss of the reconfigurable monolithic bandstop filter at 8, 10, 13, and 15 GHz.

The RF power handling capability was also tested with a 8360L Series Swept Signal Generator and a Power Amplifier Module; it was found that the filter can handle up to 30 dBm (1 watt).

## *4.5 Conclusions*

This chapter presents a monolithic reconfigurable bandstop filter utilizing the capacitive RF MEMS switches operating from 8-15 GHz. The measured results from the reconfigurable filter with the MEMS switches were compared with the measured results from a group of four individual bandstop filters with perfect open/short circuits for the ideal model of the MEMS switches; they are also compared to the simulated results. The differences between these responses were thoroughly studied. The measured results show that the rejection

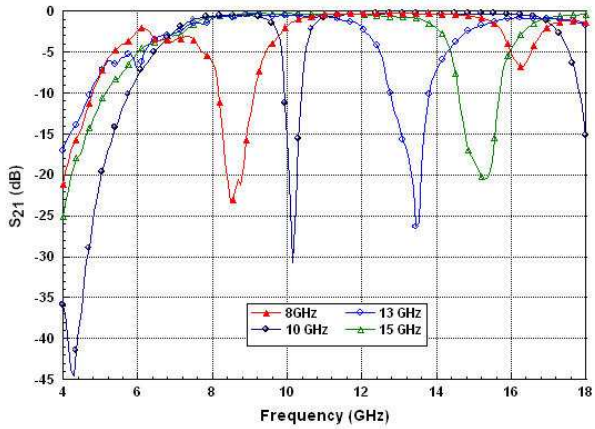



**Figure 61:** Measured composite results of the monolithic tunable filter with MEMS switches

at the notch ranges from -20 dB to -27 dB at the different resonant frequencies, while at the passband, the insertion loss is around 0.5 dB. This tunable filter can be used in future intelligent RF front-end systems for wireless communication and radar systems. It is the first step towards more mature reconfigurable/tunable bandstop filter designs with RF MEMS switches.

# CHAPTER V

# X-BAND RECONFIGURABLE IMPEDANCE TUNER FOR CLASS-E POWER AMPLIFIERS

## *5.1 Motivation*

This chapter presents an X-band monolithic impedance tuner based on microstrip transmission line, on a silicon substrate using DC contact MEMS switches, for maximizing the efficiency of class-E power amplifiers. The topology chosen is a microstrip based double stub tuner [26]. The reason to chose this one over single stub or triple stub is as follows: For single stub tuner, it requires a variable distance between the microstrip stub and the load to match a certain range of impedances, but practically it's very difficult to achieve this; while a triple stub tuner will cover the entire Smith chart, when the design requirement is not for the complete Smith chart, it will make the design more complicated. The double stub tuner has the disadvantage of not covering the complete Smith chart, but when the impedance requirement is at certain range, the great advantage of this type of matching network is it has the fixed distance (microstrip transmission line length) between the load and the open- or short-circuited stubs. The open-circuited stub was used due to its ease of modeling and fabrication, since the short circuited stub requires a via to connect to the microstrip ground plane at the back side of the wafer, which makes the fabrication process more complicated and increases the fabrication cost.

For this project, a range of impedances was given from the measured data of X-band class-E power amplifiers. The goal of the tunable impedance tuner is to cover the range of the output impedances of the power amplifier, so that when any external or internal condition changes, such as, current drifting or temperature change, etc., the tunable matching network will be able to keep track of the changes and maintain the highest possible efficiency at all conditions.

The application for the tuner presented in this chapter is efficiency optimization of hybrid ultra-high efficiency X-band PAs [20]. In this mode of operation, the active device is driven hard into saturation, and small device-to-device and parasitic variations have a large effect on efficiency. A load-pull technique combined with measurements on around 30 hybrid class-E 10 GHz PAs determines the optimal output impedances range required of the output tuner.

The tuner uses DC contact MEMS switches and microstrip radial stubs, it has a very low loss and therefore does not degrade the PA efficiency [47].

The tuners have been fabricated in two different configurations: one is the tuners are monolithically built with the rest of the circuitry for on-wafer measurements. They utilize the CPW to microstrip transitions developed from Chapter 2; the other is a set of single tuners without CPW to microstrip transitions. They are diced from the same wafer and wire bonded to the power amplifiers for power measurements.

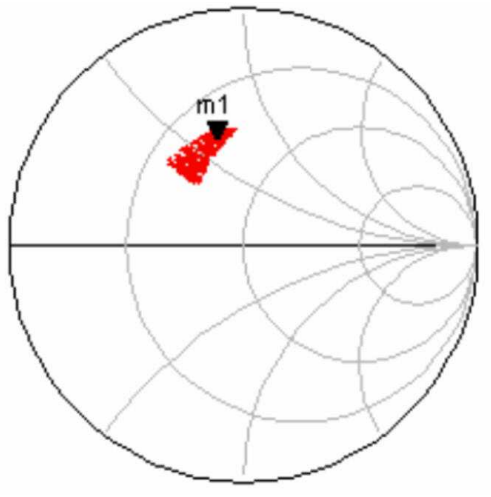
## *5.2 Impedances for High Efficiency Amplifiers*

Class-E switched mode of operation has recently gained a lot of attention at different frequency ranges [20]. In this class of operation, the transistor is operated as a switch in such a way that the current and voltage time waveforms overlap minimally during a period. Details on the design of microwave class-E PAs is given, for example, in [20]. The optimal class-E load impedance for the transistor with the given output capacitance $C_{OUT}$ can be calculated from Equation (13) [20]:

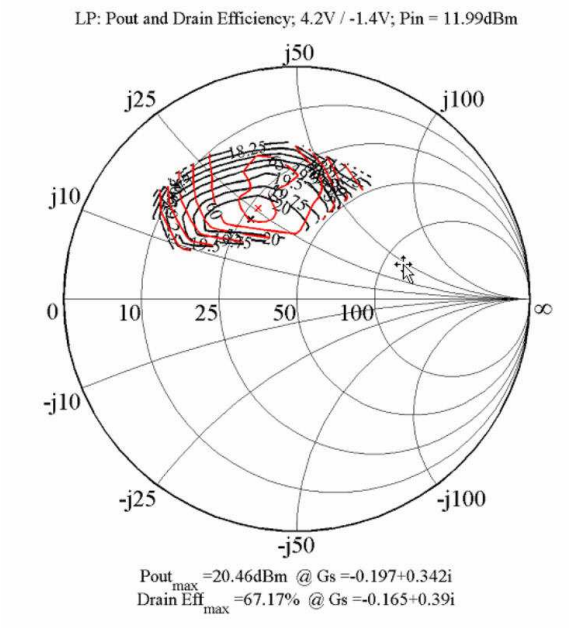
$$Z_E = \frac{0.28}{\omega_s C_{OUT}} e^{j49^\circ} \tag{13}$$

where $C_{OUT}$ is an output capacitance of the active device, and $\omega_S$ is the operating (switching) frequency.

The general purpose GaAs MESFET produced by Alpha Industries Inc. is selected as the active device. Design of a class-E PA spatial combiner using this device is presented in detail in [20]. In class-E mode of operation, voltage and current stresses on the device are higher than in linear modes of operation. Taking into account the maximum device current




(a)




(b)

**Figure 62:** (a) *Output impedance variation of class-E PA based on measurements of 30 amplifiers fabricated with devices from the same batch in identical hybrid circuits. (b) *Measured load-pull data for optimal efficiency and output power of a MESFET device integrated in a hybrid that enables direct MEMS tuner integration.
*This data is provided by the University of Colorado.

and voltage ratings, an amplifier designed with such a MESFET is capable of operating in sub-optimal class-E mode [50], but still with expected high drain efficiency, on the order of 60-70%. However, due to the relatively low linear gain of the device, and the fact that it will operate deep in compression (more than 3 dB), the PAE is 50-60%. The first step in class-E amplifier design is determination of the device output capacitance necessary for the optimal output impedance calculation (Equation (13)). If the nonlinear model of the active device is not known, a good initial estimate for the output capacitance can be obtained from the measured s-parameters. Converting s- to y-parameters and using a simple "$\pi$" linear model for the device, the output capacitance for the selected MESFET is found to be $C_{OUT} = 0.11$ pF.

From Equation (13) it can be observed that the output capacitance of the device has a large impact on the optimal impedance that is required for the high-efficiency mode of operation. Due to high levels of compression, this capacitance is nonlinear and varies from device to device. Parasitics due to hybrid integration also affect the value of the output capacitance, and therefore the optimal output impedance. For example, when $C_{OUT}$ of the device varies over a 20% range from the nominal value, $C_{OUTNOM} = 0.107$ pF, the values become $C_{OUTMIN} = 0.0856$ pF, $C_{OUTMAX} = 0.1284$ pF. The resulting output impedances for class-E operation are obtained to be as in (14) and (15):

$$Z_{EMAX} = (34.1 + j39.3)\Omega \tag{14}$$

$$Z_{EMIN} = (22.7 + j26.2)\Omega \tag{15}$$

while the nominal impedance from Equation (13) is $Z_{ENOM} = (27.3 + \text{j}31.5)\ \Omega$.

In order to determine amplifier repeatability and robustness of the fabrication process, about 30 amplifiers were made and measured. The impedance variation results are summarized in Figure 62(a). Figure 62(b) shows the contour for power amplifier efficiency. This data is provided by the University of Colorado.

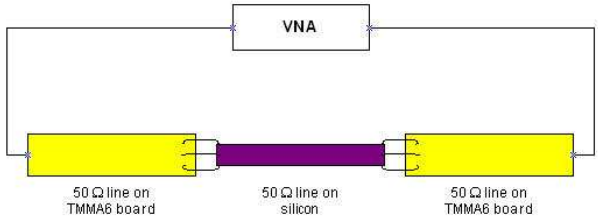



**Figure 63:** Measurement setup diagram for the subtraction of the wire bond discontinuity

## *5.3 Discontinuities from Wire Bond*

Before we move into the tuner design, there is one parameter that has to be considered, which affects not only the output impedance of the power amplifiers but also the impedances of the tuners. It's the discontinuity from the wire bond, which was used to connect both ports (50 Ω transmission lines) of the tuners to the output of the power amplifiers and the 50 Ω transmission line on the TMM6 board. The discontinuities should be considered in order to accurately generate the impedances of the tuner in the simulations.

To acquire the discontinuity data, some 50 Ω microstrip lines with the length of 5 mm were fabricated and wire bonded to 50 Ω microstrip lines on TMM6 board on both ports, then the s-parameters were measured with TRL calibration method. By de-embedding the length of the microstrip lines on the TMM6 board, and with the known characteristic of the 50 Ω line on the silicon wafer, the discontinuity data can be subtracted. The measurement setup is shown in Figure 63.

The measured s-parameters of the discontinuities caused by the wire bond are shown in APPENDIX C.

With the wire bond on the power amplifier output port, it was found that the nominal output impedance was adjusted to 34 + j37 Ω. This value will be used for the tuner design.

## *5.4 Tuner Design and DC Bias Lines Implementation*

### 5.4.1 Tuner Design

A double stub tuner design procedure is described in [26]. The design procedure for a reconfigurable double stub tuner is as follows: first, a double stub tuner was designed with

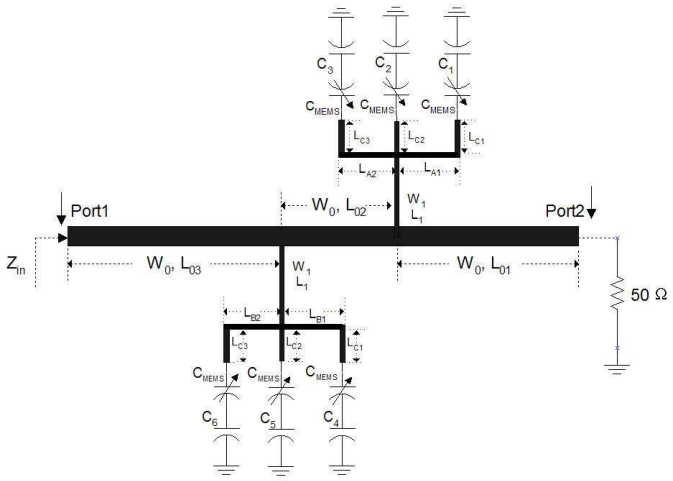



**Figure 64:** Schematic of tuner with digital capacitor $C_{MEMS}$ and fixed capacitors and fixed microstrip transmission lines

the fixed stub length to provide the nominal impedance required by the power amplifier, which is 34+j37 Ω. Next, the tuner with nominal stub lengths was redesigned, each stub was split into three paths with variable digital capacitors connected to the fixed capacitors and the fixed microstrip transmission lines. Thus, a total of $2^6 = 64$ different combinations or impedances will be generated. The schematic is shown in Figure 64.

In Figure 64, $W_0$ is the physical width of microstrip transmission feed line which is calculated with Agilent ADS LineCalc function, given that the characteristic impedance of the line is 50 Ω, and the substrate used is a 400$\mu$m silicon wafer with $\epsilon_r = 11.7$, and resistivity $\rho >$ 20,000 Ω-cm. $L_{01}$ and $L_{03}$ are the distances between the stubs and termination ports, where port2 is connected to a 50 Ω resistor which is equivalent to the input impedance of an external antenna; and port1 shows the input impedance ($Z_{in}$) seen into the tuner, which is variable. Since the characteristic impedance of the RF line is 50 Ω and this line is connected to a 50 Ω resistor, based on (16), it can be easily found that the value of $L_{01}$ will not affect the input impedance or $Z_{in}$ at port1. On the other hand, $L_{03}$ will greatly affect $Z_{in}$ (16).

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan(\beta l)}{Z_0 + jZ_L \tan(\beta l)} \tag{16}$$

Where $Z_0$ is the characteristic impedance, $Z_L$ is the load impedance, $\beta$ is the propagation constant, and $\ell$ is the physical distance from load to input impedance, and $\beta$ is the electrical

length from load to $Z_{in}$.

Also in Figure 64, $L_{02}$ is the distance between two stubs, which is another factor that affects the input impedance at port1 ($Z_{in}$). $W_1$ is the width of the stub which originally was chosen to be the same as $W_0$, which is 330 $\mu$m. In the final design, it was changed to be 110 $\mu$m to the same as that of the center signal width of the MEMS switches, in order to reduce the discontinuity, thus, reduce the tuner insertion loss. In each sub-circuit for both of the stubs, there are three $C_{MEMS}$, which denotes the value of the MEMS switch at the on- or off-state. Since the DC contact MEMS switches were used in the design, as it was shown in Chapter 3, this value is 12 fF for the off-capacitance, and 0.5 $\Omega$ for the on-resistance. Besides the $C_{MEMS}$ in each sub-circuit, there are three other fixed capacitors as $C_1$, $C_2$, $C_3$ and $C_4$, $C_5$, $C_6$ connected to each of the $C_{MEMS}$, respectively. These capacitors are used to generate the desired reactances, so that the tuner will produce the required input impedances at port1. They are used in the schematic simulation to find the initial values of reactances, and then they are replaced with certain fixed microstrip radial stubs, which provide the same reactances.

Simulations were done using two different tools in Agilent ADS: one was done with the schematic simulator, and the other one done with the EM simulator Agilent Momentum (method of moment). It was found that the results from the schematic simulation has some frequency offset from that of the Momentum simulations, this is because the microstrip transmission line model is different in both simulators. The full wave simulator (Momentum) simulates what it sees in the layout window, it includes all the fringing effects, discontinuities and radiations, but non of those effect are considered in the schematic simulator. The purpose of using schematic simulator is to get a good starting point of the tuner design.

The values of the fixed capacitors are shown in Table 9:

Based on the values in Table 9, the reactance produced by each capacitor was calculated as in (17) to convert to microstrip open-circuited stubs:

$$\frac{1}{j\omega C} = -jZ_0 \cot(\beta\ell) \tag{17}$$

**Table 9:** The required equivalent capacitances for the fixed lumped components

| $C_6$ (fF) | $C_5$ (fF) | $C_4$ (fF) | $C_3$ (fF) | $C_2$ (fF) | $C_1$ (fF) |
|---|---|---|---|---|---|
| 346 | 322 | 490 | 315 | 1020 | 390 |

with $W_0 = 330$ $\mu$m, $L_{01} = 668$ $\mu$m, $L_{02} = 668$ $\mu$m, $L_{03} = 668$ $\mu$m, $W_1 = W_0$, $L_1 = 2026$ $\mu$m, $L_{A1} = L_{A2} = 310$ $\mu$m, $L_{B1} = L_{B2} = 310$ $\mu$m, $L_{C1} = L_{C2} = L_{C3} = 580$ $\mu$m.

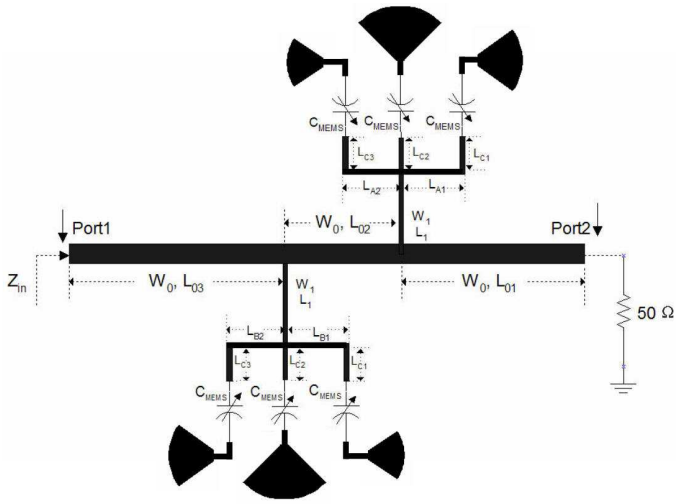



**Figure 65:** Schematic of tuner with digital capacitor $C_{MEMS}$ and microstrip radial stubs

Each fixed capacitor was then replaced by a radial stub that has the same reactance. The new schematic is shown in Figure 65. So far, a tunable impedance tuner with digital variable capacitors has been designed. By selecting the $C_{MEMS}$ as the 12 fF or 0.5 Ω, different microstrip radial stubs can be selected electrically, thus, different impedances are generated at the input port1 (port1) of the impedance tuner.

In order to design a reconfigurable impedance tuner with DC contact MEMS switches and monolithically built with the rest of the circuitry, the digital variable capacitors $C_{MEMS}$ were first replaced with the perfect open or short for the off- or on-state of the MEMS switches, respectively. Then, these perfect open or short connections were replaced by the real DC contact MEMS switches. The complete layout is shown in Figure 66.

As shown in Figure 66, there are totally six DC contact MEMS switches used for the tuner simulations in Agilent Momentum, which are named as SWn (n= 1, 2, 3, 4, 5, 6).

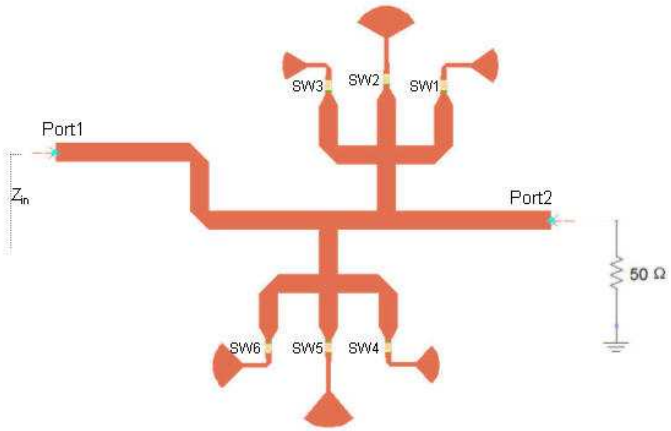



**Figure 66:** Tuner layout with DC contact RF MEMS switches

Since each SWn has two states, so, a total of $2^6 = 64$ different combinations (or impedances) will be generated. To consistently name the different combinations in the same order, a numbering convention was adopted as below:

SW6 SW5 SW4 SW3 SW2 SW1

For simplicity, to record all the different combinations with respect to different states of the MEMS switches, when the MEMS switches are at the on-state, they are symbolized as number "1"; on the other hand, when the switches are at the off-state, they are represented as number "0". For example, if SW1 and SW4 are at the on-state, while all the other switches at the off-state, the combination of the states of the MEMS switches is written as:

0 0 1 0 0 1

The simulated impedance range at 10 GHz is shown in the Smith Chart in Figure 67. In Figure 67, the marker m4 is where the nominal impedance is 33.5+j33.8 Ω; this is little bit off from the requirement (34+j37 Ω), but it is close enough for a good match. The total simulated range for the real part is from 0.63 to 57 Ω, while for the imaginary part is from -7.5 to 51.8 Ω.

So far, an individual microstrip transmission line based impedance tuner with DC contact MEMS switches has been designed. In order to facilitate the on-wafer measurements, the CPW RF probe pad to microstrip transition has to be added to both sides of the tuner

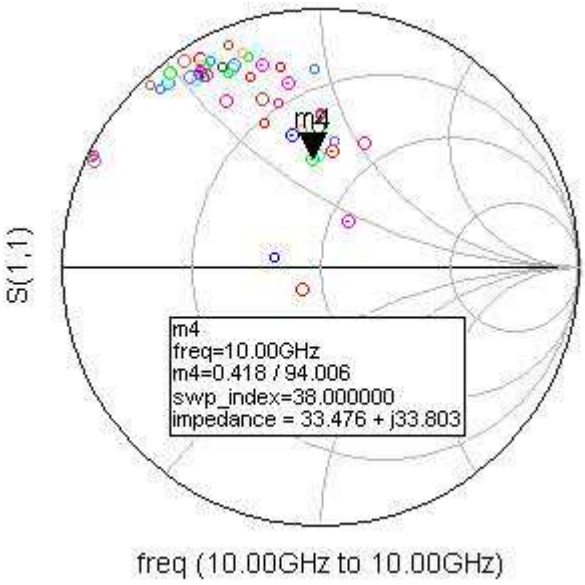



**Figure 67:** Simulated impedance tuning range at 10 GHz shown in Smith Chart

feed line. The configuration of the impedance tuner with the via-less transition is shown in Figure 68.

As shown in Figure 68, the CPW RF probe pads at both sides were used for RF probing purpose. In the TRL calibration set, the total length of two CPW to microstrip transition with back to back configuration is set as the total length of the through line. After the TRL calibration, the length of the through line was de-embeded, and the reference plane was set at the end of transition at microstrip line side: the "reference plane A" and "reference plane B" in Figure 68. This ensures that the reference planes of the individual impedance tuner are at exactly the same reference planes as that of the tuner for on-wafer measurements.

### 5.4.2 DC Bias Lines Implementation

In order to appropriately operate the impedance tuner, more specifically the MEMS switches, the DC bias lines have to be considered and carefully implemented, in order to provide the DC path to the MEMS switches, as well as not to degrade the RF performance.

As shown in Chapter 3 section 2, to actuate a single DC contact MEMS switch there are three connections needed for the DC applications: one is to the membrane or the MEMS switch input transmission line; the second is to the bottom contact metal or the

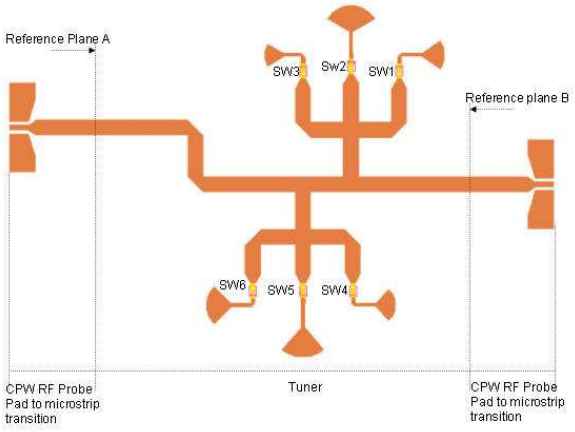



**Figure 68:** Tuner layout with CPW RF probe pad to microstrip transition for on-wafer measurement

output transmission line, which has the same potential as that of the membrane; and third one is to the bottom electrode. Since the MEMS switches used for the impedance tuner are monolithically integrated with the rest of the circuitry, different DC bias lines have to be laid out. Referring to Figure **??**, all of the six MEMS switches have one common connection, which connects to the membrane of all the MEMS switches, through the 50 Ω RF transmission line. So, one DC bias line can be connected to the RF line to provide the common DC ground to the membrane of all the MEMS switches. While for the bottom contact metal (which connects to the microstrip radial stubs) of all the MEMS switches, they are all separate from one and another, thus, different DC bias lines have to be connected to those radial stubs as the second DC ground. To actuate the MEMS switches, a voltage (positive or negative) has to be supplied to the bottom electrode, thus, a different DC voltage path for the bottom electrode of each MEMS switch has to be provided. This will result in a total of 11 DC bias lines if each pad is separate. Considering that all the DC grounds can be connected together, since they have the same potential, the total number of the DC bias line pads can be reduced.

Each DC bias line consists of two parts: one is the highly resistive material closely connected to the three different parts of the MEMS switches, which is formed by using a chemical etching process; the other one is the thin film of gold which is formed by a lift-off process. Both of them are patterned underneath the dielectric material $Si_3N_4$ and are

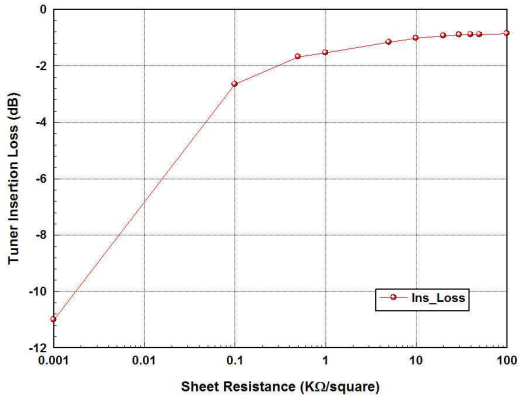



**Figure 69:** The simulated tuner insertion loss vs. the sheet resistance of the DC bias lines

protected from subsequent fabrication process. The purpose of the highly resistive material is to provide a very high impedance of the line to prevent the RF leakage, while the gold line connected to it also connects to the DC probe pad, to provide the DC path. The thin layer of highly resistive material was formed with the method of combustion chemical vapor deposition (CCVD) with the assistant of nGimat.

There are two types of highly resistive materials used for this purpose, which are Indium Tin Oxide (ITO) and Aluminum doped Zinc Oxide (AZO). Experiments with ITO were first conducted and it was found the sheet resistance of ITO degrades with the exposure to the moisture in the air. In the worst case, a high resistivity silicon wafer (covered with 1 $\mu$m of $SiO_2$) deposited with ITO was first measured to have a sheet resistant of around 20 KΩ/square. But after the fabrication was done, the DC bias lines on the wafer were measured and the sheet resistance was calculated and found to be less than 1 KΩ/squre. As a result, the tuner insertion loss had increased. In order to maintain or to have a relatively stable sheet resistance, an alternative material AZO was chosen. The experiments showed a better results for the DC bias lines from this material.

To study the loading effects of the DC bias lines, the simulations of the tuner with the combinations of the MEMS switch states that provide the nominal impedance were performed, with varied sheet resistance of the highly resistive material. The results are shown in Figure 69.

Figure 69 clearly shows that when the resistive material sheet resistance used for the DC bias line is greater than 10 KΩ/square, the tuner insertion loss is about the same which is around 1 dB; the tuner insertion loss increases when the sheet resistance decreases. And, when the sheet resistance dropped below 1 KΩ/square, the insertion loss of the tuner starts to increase exponentially. Since the measurement shows that the sheet resistance of the DC bias line with ITO is only around 0.7 KΩ/square after the fabrication (5 KΩ/square to 10 KΩ/square prior to the fabrication), it can be seen from the simulation that the tuner insertion loss increases from about 0.9 dB to 1.9 dB. Considering the non-uniformity of the deposited ITO on the silicon substrate, some DC bias lines might have even lower sheet resistance than 0.7 KΩ/square which will definitely degrade the tuner performance.

Thus, in order to improve the tuner loss, a much higher sheet resistance of the DC bias lines has to be provided. AZO is proposed to use for the implementation of the DC bias lines. With the assistance of nGimat, it has been shown that this material can be deposited to achieve much higher sheet resistance, and maintain a relatively stable performance. With a much higher initial sheet resistance of around 200 KΩ/square, the resistive part of the DC bias line is very much shortened. The width of the line is 20 $\mu$m, while the length is 400 $\mu$m, which has the total effective length of 20 squares. With this initial value, It is expected to see about 4 MΩ DC resistance, but the actual measured resistance ranging from 200 KΩ to 500 KΩ. Even though the resistance still changes a lot which is suspected both due to the non-uniform deposition and unstableness of AZO, it provides a sufficient RF energy blockage.

The deposition of both the ITO and AZO was done by nGimat using combustion chemical vapor deposition (CCVD). One common issue about this technique is the deposited highly resistive material (ITO or AZO) is very non-uniform, with the sheet resistance of the material around the edge of the wafer much higher than that of the material in the center of the wafer. So, in order to achieve better results for the DC bias lines, the highly resistive material and the thin layer of gold were pattered alternatively. As an example, the DC bias lines layout for “SW5” and “SW6” (in Figure 68) is shown in Figure 70.

Figure 70 shows the DC bias lines’ layout for SW5 and SW6. The highly resistive

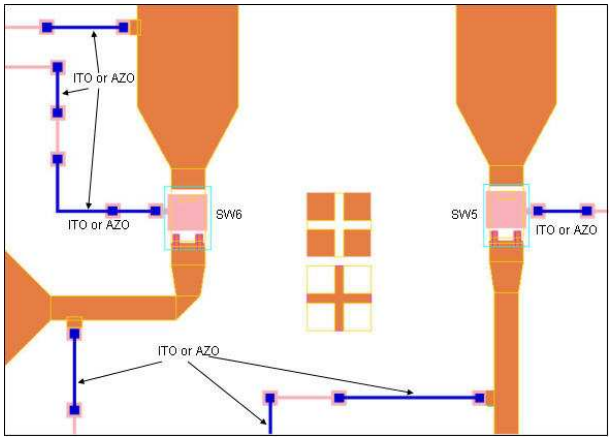



**Figure 70:** The close-up of the DC bias lines for SW5 and SW6

material (ITO or AZO) was pointed out in the figure (blue lines), while the other section of the lines alternatively connected with them are the thin gold lines (pink lines). The width of the ITO or AZO line is 20 $\mu$m, and the total length is 1000 $\mu$m, which gives effective length of 50 squares. With the deposited sheet resistance of the ITO or AZO around 20 K$\Omega$/square, we can get a DC bias line with a DC resistance of about 1M$\Omega$. This is sufficient to prevent the RF energy leakage through the DC bias lines. If the sheet resistance is higher, a shorter line of the highly resistive material (ITO or AZO) can be used.

The layout of tuner with the CPW RF probe to microstrip transitions and the DC bias lines is shown in Figure 71. It shows that joining the DC ground pads together, the total DC probe pads are reduced to 8 pads. Two DC probe cards with a 150 $\mu$m pitch and two individual DC probes can be used to actuate all the MEMS switches. For the on-wafer measurements, the common DC ground which connects to the membranes of all the MEMS switches can be provided through the RF probes using two DC bias Tees.

For the individual tuners that are diced from the same wafer and wire bonded to the power amplifier, the DC bias lines also have to be properly designed. Since all the DC probe pads were also wire bonded to the DC lines on the TMM6 board, they must be all separated from one another. The DC pads on the silicon wafer were designed as 500 $\mu$m x 500 $\mu$m square pads. The layout is shown in Figure 72. Port1 and port2 are at the same positions with the “reference plane A” and “reference plane B” for the tuner with the on-wafer measurement configuration.

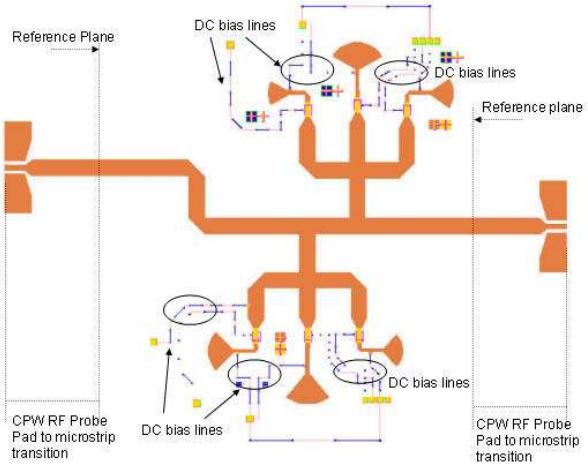



**Figure 71:** The tuner layout with DC bias lines for DC contact MEMS switch and CPW RF probe pad to microstrip transition

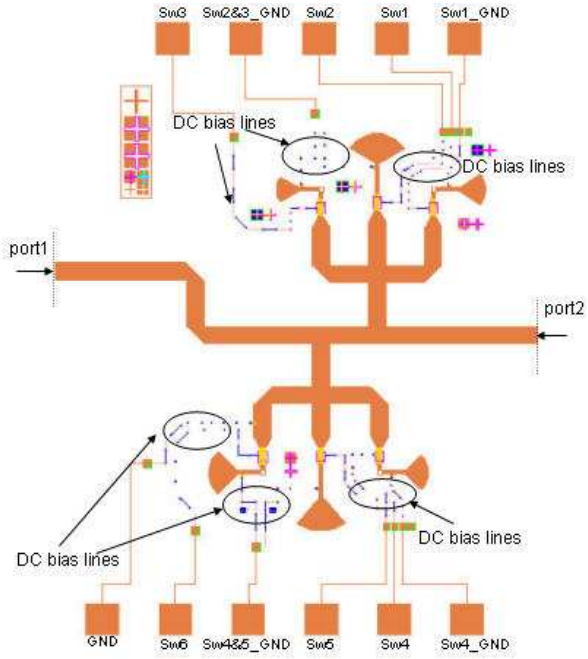



**Figure 72:** The individual tuner layout with DC bias lines for DC contact MEMS switch.

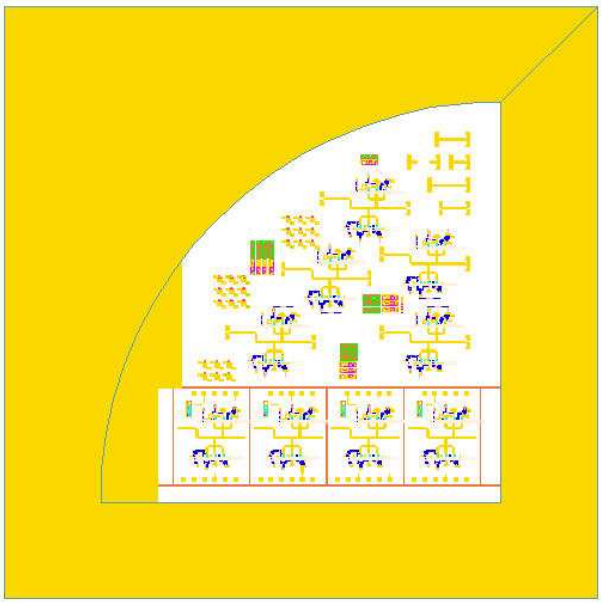


**Figure 73:** The impedance tuner mask layout for fabrication

## *5.5 Tuner Layout Generation and Fabrication Process Flow Development*

Prior to fabrication, a mask layout has to be generated carefully. Since all the fabrication will be done on a $\frac{1}{4}$ piece of a $4''$ wafer, which is a relatively small space, it is necessary to put as many as possible testing devices on the same wafer in case of yield issues or for the purpose of repeatability testing. On the other hand, the distance between each device has to be well planned to avoid the cross talk or coupling issues. A good mask layout is very inclusive and complete to include all possible devices at different stages in order to trace back the problems, if anything wrong is detected in the final device measurement. Considering this, all five following devices were included in the mask layout: the single DC contact MEMS switch in order to characterize the RF MEMS performance; two sections of DC bias lines to characterize the sheet resistance of ITO or AZO; The TRL calibration lines for on-wafer measurement; the impedance tuners with the CPW RF probe pads to microstrip transitions for comparison purpose between the measurements and simulations; individual tuners that will be diced and wire bonded to the power amplifiers. This layout is shown in Figure 73. Mask layout in this picture contains 7 different layers to complete the final fabrication.

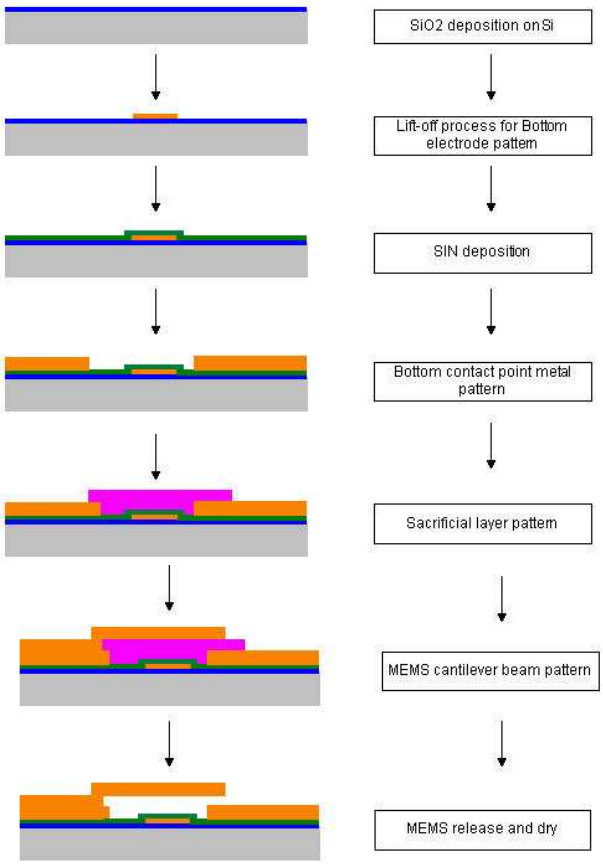



**Figure 74:** The impedance tuner Fabrication process flow

The fabrication was done on a high resistivity Silicon wafer with $\epsilon_r = 11.7$, $\rho > 10{,}000$ Ω-cm, and a thickness of 400 $\mu$m. The fabrication process flow is shown in Figure 74, and the detailed fabrication process can be found in Appendix IV.

In summary, the fabrication process includes the following steps: 1) The resistive material was deposited with CCVD (combustion chemical vapor deposition) and patterned to provide the DC bias line for the tuner. The resistor was measured to be around 500 KΩ. 2) The bottom electrode layer was formed with 2000 $\mathring{A}$ gold with E-beam evaporator and then patterned. 3) A thin layer of silicon nitride (2500 $\mathring{A}$) was then deposited with PECVD (Plasma therm chemical vapor deposition), and then patterned with plasma therm RIE (Reactive Ion Etch) to provide the DC contact point. 4) The first metal layer was patterned and electro-plated with gold to 1 $\mu$m thick to provide the contact point between the membrane and this metal layer. 5) The backside of the wafer was metallized with gold

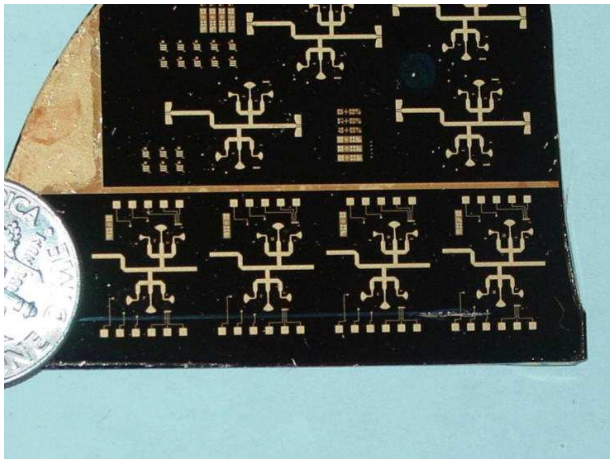


**Figure 75:** Fabricated impedance tuners on a quarter piece of a 4" wafer

to 3 $\mu$m. 6) The sacrificial layer was patterned with photo resist with a thickness of around 2 $\mu$m. 7) The membrane layer was electro-plated with gold to a thickness of 2 to 2.5 $\mu$m to provide about 4 times the skin depth; it was then released with the photo resist stripper. 8) Finally, the wafer was dried with critical point dryer to prevent the stiction problem.

The picture of the fabricated circuit is shown in Figure 75. As it can be seen from Figure 75, there is a straight gold line at the lower part of the wafer which is patterned to separate the different devices above and below it. The circuits above the line are for the on-wafer measurement; the four microstrip based single tuners below the line will be diced and then assembled with the power amplifier. A picture of the diced single tuner is shown in Figure 76.

There are a lot of aspects that have to be considered at the same time to assure a successful fabrication, and there are a lot more challenges and difficulties coping with them since this is a much more complicated fabrication process than that for the tunable bandstop filters. Below are some highlights of them:

1) In order to minimize the dielectric charging problem, the sacrificial layer has been exposed twice to form a small dimple on the top of the sacrificial layer which is not shown in Figure 12. The size and different exposure time has to be well calculated so that a dimple will be formed but will not be too much so that the cantilever beam will be in contact with the $Si3N_4$ layer on top of bottom electrode.

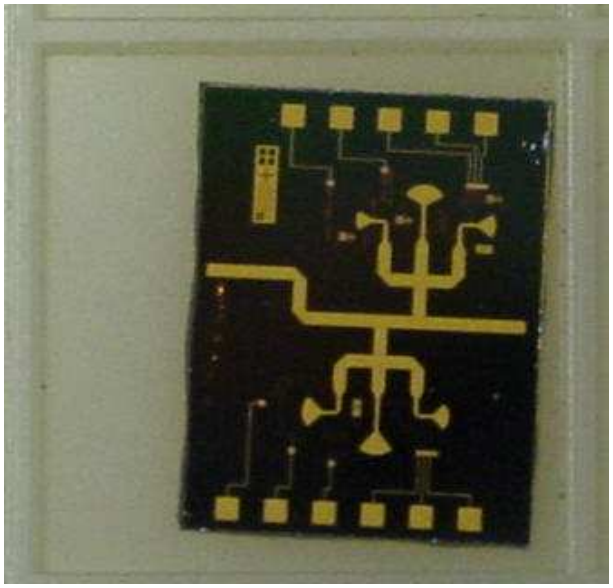


**Figure 76:** The picture of fabricated individual tuner on silicon wafer

2) The timing for the individual tuners' dicing is a very important factor for a successful fabrication. There are three possible options as to when to dice the wafer:

Option 1: The wafer is diced prior to the membrane release. This was done after the fabrication of the bottom contact metal completion and before the sacrificial layer was patterned;

Option 2: The wafer is diced prior to the membrane release but after the cantilever beam layer was patterned and electro-plated.

Option 3: The third option is the post-release dicing, which is done after the total fabrication is complete.

Among all the options, the second one is the best way since after dicing, the only work has to be done is to release the membrane. The first option can also be used, but it requires cumbersome fabrication work after dicing since each single tuner has to been handled individually. The disadvantage is it normally results in a non-uniform gold plating and different thickness/metal stress of the membrane. As a result, a large variation of the actuation voltages for different single tuners is produced. The third option is not a very good one, since the dicing creates dusts or particles on the wafer. In order to clean the surface of the wafer, a very low pressure nitrogen gun needs to be used which is not very

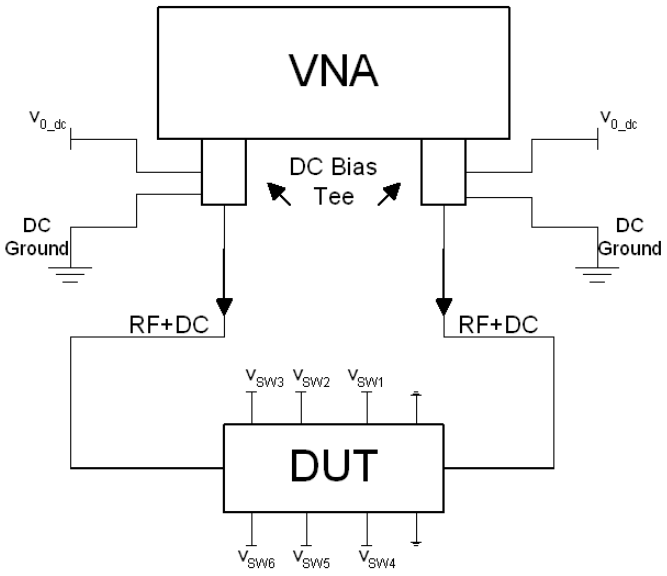



**Figure 77:** The measurement setup diagram for the impedance tuner with on-wafer measurement configuration

sufficient. In the worst case, some of the membranes of the MEMS switches will be blown away.

## *5.6 Measurements and Results*

There are two measurement setups for the tuners: The first one is for the on-wafer measurement; the second one is for the measurement of an individual tuner wire bonded to the TMM6 board.

### 5.6.1 On-Wafer Measurements

The on-wafer measurement was performed with an Agilent 8510C network analyzer using Cascade probe station, and GGB Picoprobes. The DC contact MEMS switches were activated using five Cascade DC probes, one DC probe card with a pitch of 150 $\mu$m, and two DC bias Tees which are connected to the VNA. The setup is shown in Figure 77.

The "DUT" in Figure 77 is the impedance tuner that has the CPW RF probe pad to microstrip transitions for on-wafer measurements. The common DC ground connected to the membranes of all six MEMS switches was supplied through the DC bias Tees at both ports of the VNA. The bottom contact metals were also connected to the DC ground

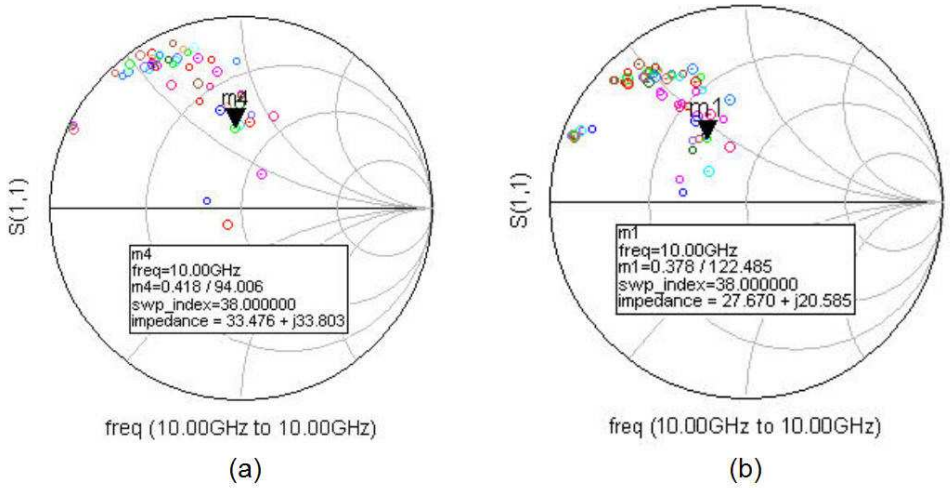



**Figure 78:** (a) Simulated impedance tuning range (b) Measured impedance tuning range from on-wafer measurement

through external DC probes, and the voltages to the bottom electrode of all six MEMS switches were supplied through external DC probes (including DC probe cards and the single DC probes). The measured actuation voltage was found to be 30-35 volts.

The measured results from the tuner with the on-wafer measurement configuration is shown in Figure 78(b), and are compared to the simulated results in Figure 78(a).

Compared the measured results to the simulated results in Figure 78, two trends can be found from the data: The fist one is that all data from the measurement has rotated counter-clockwise a little bit; this is caused by some capacitive effects from the circuits. Mainly it is because the fabricated MEMS switches are not exactly the same as the simulated ones, which is reasonable due to inevitable fabrication process variations, such as metal stress, metal deposition rate, and gold plating rate, etc., As a result, membrane deformation will occur, thus, the equivalent off-state capacitance and on-state contact resistance from each MEMS switch has slightly changed. The second trend is that all the data from the measurements has moved toward the center of the Smith Chart slightly; this is caused by the fact that the fabricated impedance tuner shows some more loss than the simulated one.

### 5.6.2 Individual Tuner Assembling and Wire Bond

The measurements for the individual tuner are more complicated than for the impedance tuner with on-wafer measurement configurations. Prior to the measurements, a single tuner on the silicon wafer needs to be bonded to the fixture. The bonding process is completed by performing the following steps very carefully:

1) The first step is to build the test fixture for the individual tuners. The fixture used is aluminum, and the complete fixture contains four different parts. Two parts of the fixture are made for the TMM6 boards that have the 50 Ω transmission lines on it, one part of it is for the individual tuner on the silicon wafer, and the last one is for the TMM6 board with the power amplifier on it.

2) The second step is to bond the two TMM6 boards onto the aluminium fixture with any type of bonding material. This step is not critical as long as the board is bonded to the aluminum fixture tightly enough.

3) The third step is to connect two SMA (SubMiniature version A) connectors to the 50 Ω transmission lines on TMM6 boards bonded to the aluminum fixture. The center pin is soldered to the 50 Ω line and SMA connectors were connected and tightened to the aluminum fixture through two small screws.

4) The next step is to assemble the three parts of the aluminum fixture before the bonding of the single tuner on the silicon wafer. The assembling sequence is to have each of the fixtures with the TMM6 board with the transmission line on it on both sides, and the fixture made for the single tuner in the middle, using two long screws to connect them together and tighten them.

4) The following procedures are for the bonding of the single tuner on the silicon wafer to the aluminum fixture by using silver epoxy, which has to be done very carefully: apply the minimum amount of silver epoxy onto the fixture, and then spread it out carefully and evenly; place the single tuner on the silicon wafer onto the fixture and slightly press the edges of the wafer; move the assembled fixture on a hotplate with temperature preset at 70°C.

5) The next step is to leave the assembled tuner on the hotplate for about 10 hours

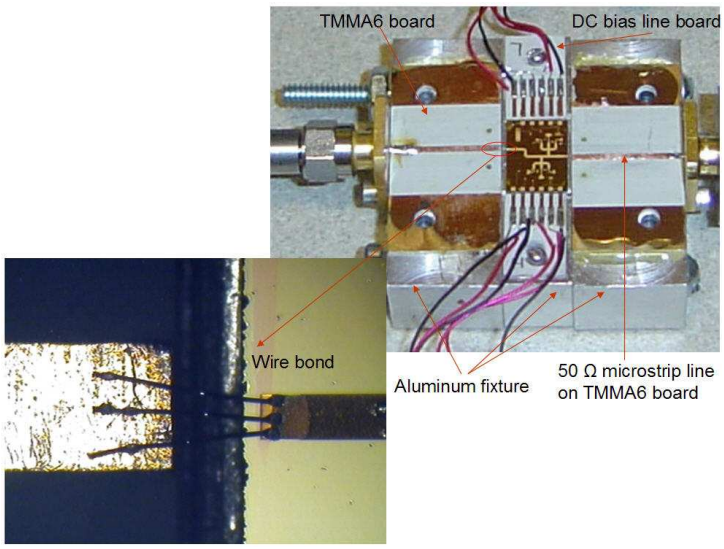



**Figure 79:** An individual impedance tuner on the silicon wafer wire bonded to the TMM6 board and the close-up of the wire bond

to slowly cure the silver epoxy. The curing temperature is very important and should not be changed at any time of the bonding process. A high bonding temperature is not recommended, since the gassing problems of the silver epoxy will occur, and as a result, the MEMS switches may have stiction problems.

6) After the tuner bonding is done, move the assembled tuner off the hotplate and let it cool down to room temperature. Then, assemble two DC boards (TMM6) on each side of the single tuner (top and bottom side), with the small screws. These two DC boards have exactly the same number of the DC probe pads on the silicon wafer for the single tuner.

7) The last step is to wire bond the tuner to the transmission lines and DC lines on the TMM6 boards. Each of the two 50 Ω RF transmission lines (input and output ports) of the single tuner on the silicon wafer was wire bonded to each of the RF transmission lines on the TMM6 boards. In order to reduce the inductance, three wires in parallel were jumped from the RF lines on the silicon wafer to the RF lines on the TMM6 boards. The 11 DC pads on the silicon wafer were wire bonded to the DC pads on the TMM6 boards afterwards. The complete configuration is shown in Figure 79.

Figure 79 shows an assembled single tuner, and the close-up for the wire bond from RF line on the TMM6 board to the RF line on the silicon wafer, with three jump wires in

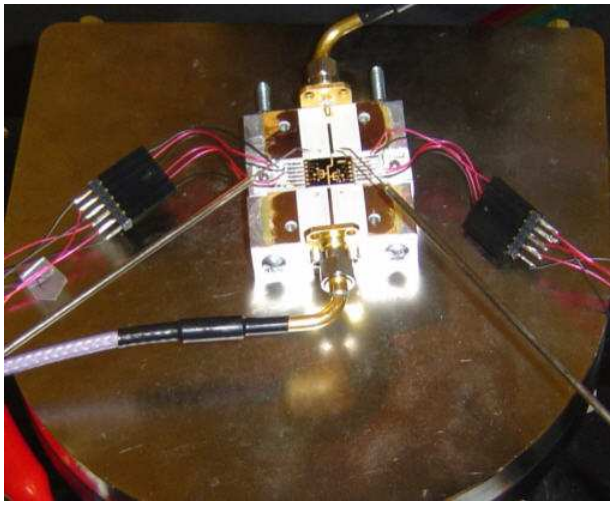


**Figure 80:** Picture for an assembled individual tuner in the middle of the measurement

parallel.

### 5.6.3 Assembled Individual Tuner Measurements

Two different measurements were performed for an assembled tuner: one is the s-parameter measurement; and the other is the power measurement, with the purpose of testing the power handling of the tuner and the MEMS switches.

#### *5.6.3.1 S-Parameter Measurement*

In order to take the s-parameters of the assembled tuner, the measurement was setup in the same way as for the measurement of the tuner with the on-wafer measurement configuration. The diagram for the measurement setup can be referred to Figure 77, with the differences of that the assembled tuner is connected to the VNA through the SMA connectors instead of the RF probes, and the DC supply (DC voltage and the DC ground) is applied through the two TMM6 DC boards wire bonded to the single tuner on the silicon wafer. The TRL calibration is done, and after deembeding, the reference plane is moved to where the wire bonds end with the other side connected to the 50 Ω line on the silicon wafer.

The picture of an assembled single tuner in the middle of measurement is shown in Figure 80.

As shown in Figure 80, the 50 Ω lines on the TMM6 board were connected to the network

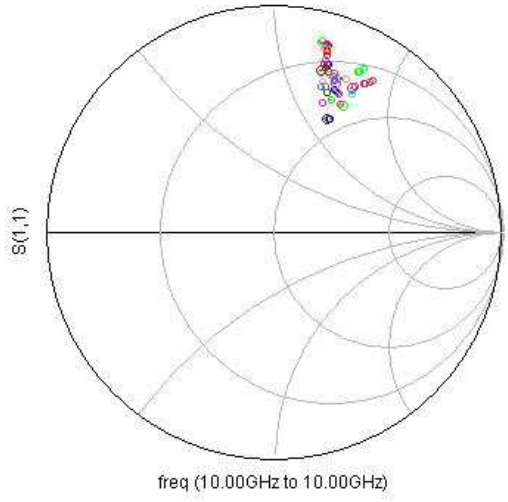



**Figure 81:** Measured impedance range from an assembled individual tuner

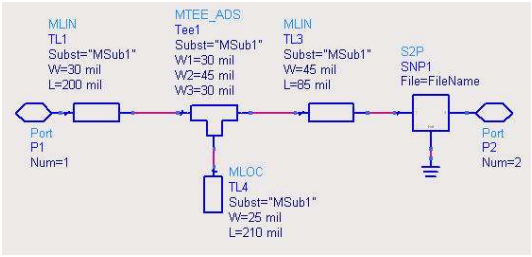



**Figure 82:** The schematic for the assembled individual tuner impedance rotation

analyzer through two RF cables. The plastic wires and DC probe in the picture provide the DC voltages needed for the MEMS switch actuation. The measurement was done with an Agilent 8510C network analyzer, the calibration method used was TRL calibration. After the calibration is done, both of the 50 Ω lines on the TMM6 boards were de-embeded, and the reference planes were set at the edge of the wire bonds on TMM6 boards side.

The s-parameters were taken, and results were plotted in the Smith Chart as shown in Figure 81. The results show that the impedances generated from the assembled tuner have moved clockwise and that the range has shrunk, this is caused by the inductance effects from the wire bonds at the both sides of the tuner. In order to move the impedance back to the required range, a single open-circuited microstrip stub is added to the output of the power amplifier on the TMM6 board. The schematic are shown in Figure 82, and the impedances after the rotation is shown in Figure 83.

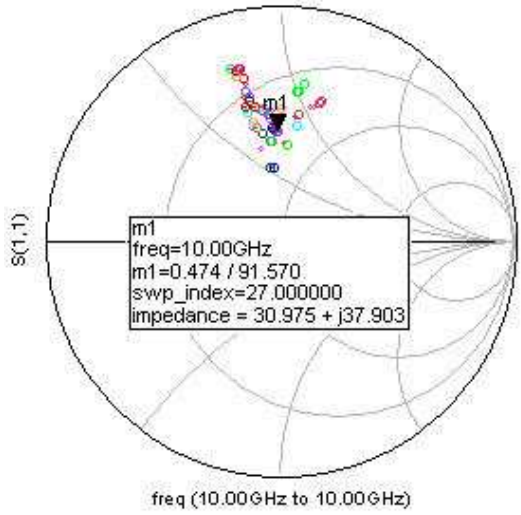



**Figure 83:** The impedances from the assembled individual tuner after the impedance rotation

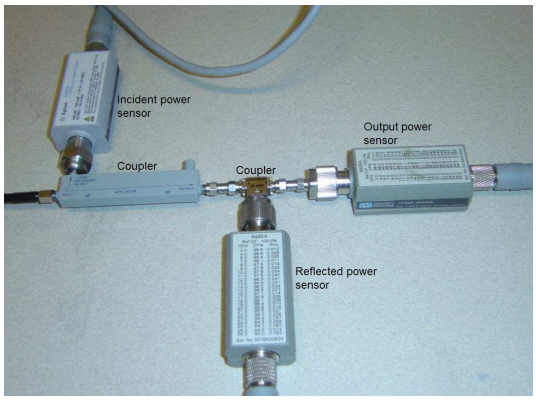



**Figure 84:** Power measurement calibration for an assembled individual tuner

#### *5.6.3.2 Power Measurement*

The power measurement was also taken for an assembled single tuner. There are two purposes for the power measurement: the first one is to find out the power handling capability of the tuner and the MEMS switches; the second one is to calculate the insertion loss of the assembled single tuner with respect of the input power and the output power. The measurement setup is shown in Figures 84 and 85.

Figure 84 shows the calibration setup for the power measurement. The coupler in the picture is used to sample the incident power, and the isolation between the reflected port and the forward port is 20 dB. The circulator is used to sample the reflected power. This

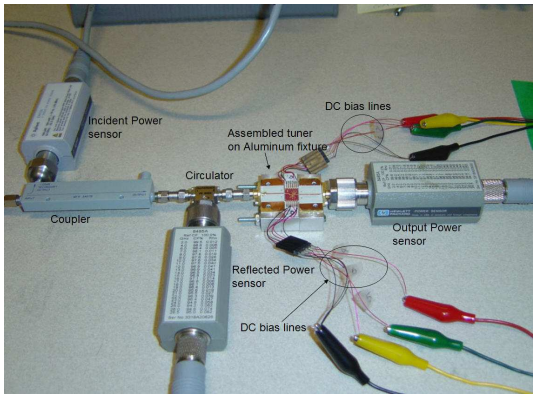



**Figure 85:** Power measurement for an assembled individual tuner

configuration is setup so that the errors from the measurement equipment are calibrated out, and we can get accurate power readings for the assembled tuner power measurement.

Figure 85 shows the power measurement setup for an assembled single tuner. Up to 1 watt incident power was put into the system to measure the reflected and the output power. With a measured tuner insertion loss of 3 dB, 0.5 watts input power actually goes through the tuner.

Only the selected states of the assembled single tuner are measured to verify the tuner loss. After the testing is done, the assembled individual tuner is sealed in a container and shipped to the University of Colorado for the power efficiency measurements.

### 5.6.4 Tuner Insertion Loss

There are different ways to characterize the loss of a network inserted in a system. Two different methods are presented in this section: one is characterized as a term "percentage loss", the other one is commonly used insertion loss.

The definition of the "percentage loss" is shown in equation (18):

$$PercentageLoss(\%) = \frac{P_{loss}}{P_{inc}} = 1 - \mid S_{11} \mid^2 - \mid S_{21} \mid^2 \tag{18}$$

Where, $P_{Loss}$ is the power loss in the tuner; $P_{inc}$ is the incident power from the power source; $S_{11}$, $S_{21}$, $S_{12}$, $S_{22}$ are the measured s-parameters of the full two port network(tuner).

The definition of the insertion loss is shown in equation (19):

$$InsertionLoss(dB) = 10\log(\frac{P_{out}}{P_{inp}}) = 10\log(\frac{\mid S_{21} \mid^2}{1- \mid S_{11} \mid^2}) \quad (19)$$

Where, $P_{out}$ is the output power from the tuner or the power delivered to the load; $P_{inp}$ is the input power delivered to the tuner, with $P_{inp} = P_{inc}$ - $P_{ref}$, where $P_{ref}$ is the reflected power from the tuner. Referring to Figure 85 for the power measurements, the incident power ($P_{inc}$) is sampled by the first coupler connected to the input of the circulator, the reflected power ($P_{ref}$) is sampled by the circulator, and output power ($P_{out}$) is monitored by the coupler connected to the output of the tuner.

Equation (18) measures the percentage loss of the inserted network (impedance tuner in this case) with respect to the incident power, or how much power lost in the tuner compared to the incident power; While the insertion loss measures the ratio of the power delivered to the load (50 Ω) to the input power delivered to the network (tuner).

For a standard 50 Ω system, $\mid S_{11} \mid^2 \sim 0$, thus, the loss from the tuner will be $1 - PercentageLoss = 1 - (1- \mid S_{11} \mid^2 - \mid S_{21} \mid^2) = \mid S_{21} \mid^2$ from equations (18), which equals to equation (19) when $\mid S_{11} \mid = 0$. But since the impedance tuner is designed as the output matching network for the power amplifier, they have complex impedances seen from port1, and 50 Ω seen from port2, thus, the term "percentage loss" won't be valid for the loss characterization using a standard 50 Ω vector network analyzer, because $\mid S_{11} \mid \neq 0$ or port1 is not matched. Instead, the insertion loss calculated from Equation (19) is used to characterize the tuner loss.

The measured tuner insertion loss from the on-wafer measurements agrees to the results from the assembled individual tuner, both were found to be about 2 dB higher than the simulated results. The nominal insertion loss from simulations is 1.2 dB, while the measured insertion loss from the on-wafer measurement is about 3.2 dB. The discrepancy between the simulations and measurements is also observed in the improved tuner design, which is studied and analyzed in the following section.

Moreover, at different impedances generated from the different combinations of the different MEMS switch state, the tuner exhibits higher loss at some states than others. By electrically choosing the appropriate combinations of the MEMS switch state, the tuner can

provide a tunable matching network for the power amplifier with an average loss of about 3 dB.

### 5.6.5 Tuner Design Improvement and Results

#### *5.6.5.1 Design Improvement*

In order to improve the tuner loss at all states, the design was slightly modified from the original one. The microstrip stub line width is changed to 110 $\mu$m from 330 $\mu$m to be the same as for the center RF line width of the RF MEMS switches, in order to reduce the discontinuity. The simulated results show the insertion loss for the combination of the MEMS switch states that give the nominal impedance is improved from 1 dB to 0.5 dB.

The highly resistive material used for the DC bias lines was also changed to AZO from ITO. As mentioned in the previous section, the electrical performance of ITO greatly degrades after the fabrication. Although the resistivity of the AZO degrades too after the complicated fabrication process, it has relatively smaller degradation compared to ITO. Further more, it is easier to achieve a higher sheet resistance than that for ITO. Thus, AZO was used as the highly resistive material for the DC bias line implementation. With a much higher initial sheet resistance of around 200 K$\Omega$/square, the total length of the resistive part of the DC bias line is very much shortened. The width of the line is still 20 $\mu$m, while the length is to 400 $\mu$m, which has the total effective length of 20 squares. with this value, it is expected to see a DC resistance of 4 M$\Omega$ after the fabrication. But due to the unstable nature of the material, the actual measured resistance varies from 500 K$\Omega$ to 800 K$\Omega$. Although the resistance still changes a lot, it can provide a sufficient RF energy block from the DC bias lines.

Figure 86 shows the close view of the DC bias lines for Sw5 and Sw6. As it can be seen, the DC bias lines are formed with two different materials connected to each other. The one placed close to the edge of the MEMS switches and the RF lines is AZO; and the other one is the thin layer of gold patterned by the lift-off process, which connects to the DC probe pad on the other side.

A fabricated wafer after dicing is shown in Figure 87, and the picture of an individual

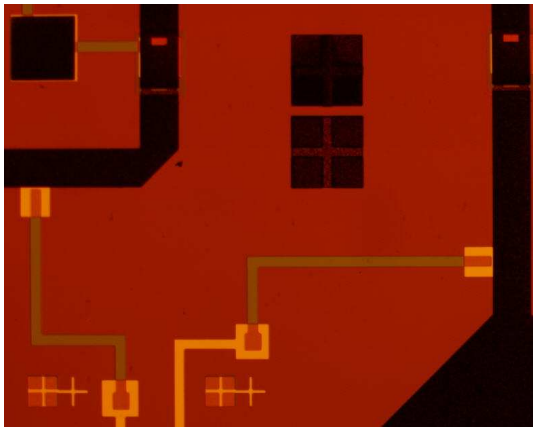


**Figure 86:** The picture of the DC bias lines for the Sw5 and Sw6 of a fabricated tuner with the improved design

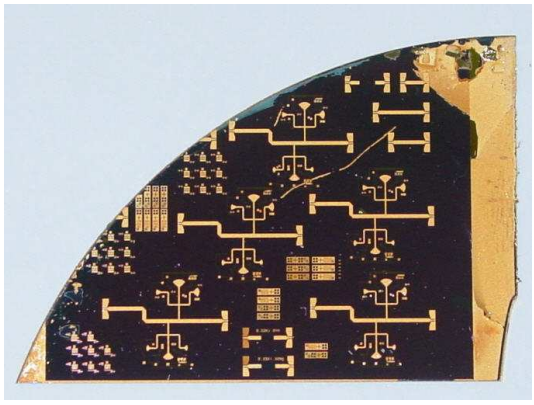


**Figure 87:** The picture of a fabricated circuit after dicing with the improved tuner design

tuner before the assembling is shown in Figure 88. In both figures, it shows that the stub width has been changed to be 110 $\mu$m, to match that of the center RF line width of the MEMS switches. The individual tuner in Figure 88 still has the same reference planes as that of the tuner with on-wafer measurement configuration shown in Figure 87. The results from simulations and measurements show that both the impedance range and the insertion loss have been improved.

#### *5.6.5.2 Simulated and Measured Results*

The measurements were taken with the same procedure as described in the previous section for both on-wafer and assembled individual tuner.

Figure 89 shows the on-wafer measurement of the tuner in the middle of the measurement

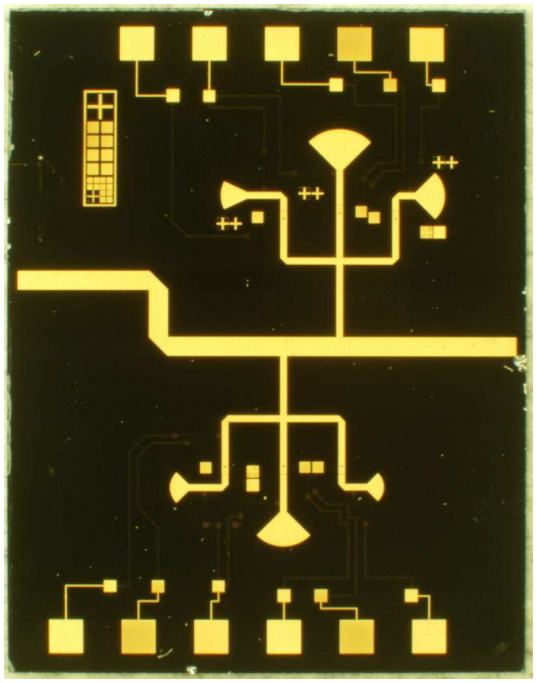


**Figure 88:** The picture of the fabricated individual impedance tuner with the improved design

process. The measurement was done by using an Agilent 8510C vector network analyzer and a Cascade probe station. In Figure 89, the two probes connected to both ports of the tuner are Cascade Pico probes with a pitch of 200 $\mu$m. The four individual probes at the bottom side of the tuner are four Cascade DC probes to provide the DC application; another individual DC probe is positioned at the upper side of the tuner to provide the DC path, one GGB Industries DC probe card with a pitch of 150 $\mu$m is also used for the DC applications.

The comparison between the simulated and the measured impedance range and the tuner insertion loss are shown in Figures 90 and 91.

Figure 90(a) shows the simulated impedance range with the improved design, and Figure 90(b) shows the impedance range from the on-wafer measurements. It can be seen from both figures, the impedance range has been changed to mostly around the nominal impedance which is 35.9 + j37.3 Ω from the simulation, with the simulated impedance range from 3.2 to 57.7 Ω for the real part, and -2.4 to 55.2 Ω for the imaginary part. The measured results show the corresponding nominal impedance has slightly shifted to 29.7 + j34 Ω, with the

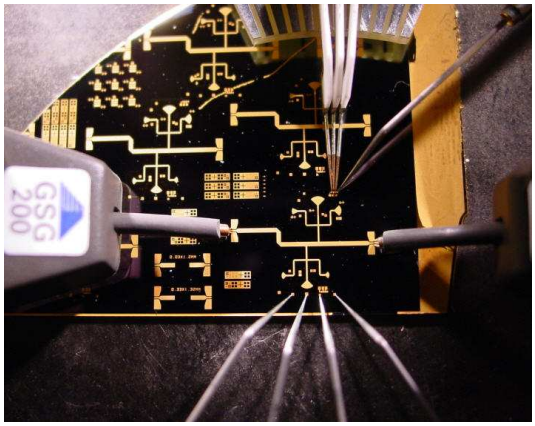
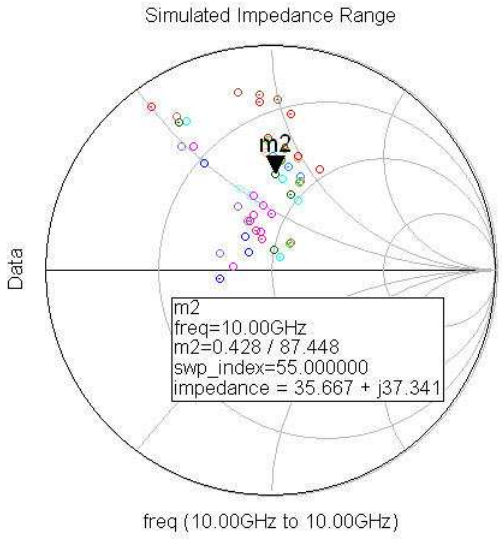



**Figure 89:** Picture of the on-wafer measurement of a tuner with the improved design

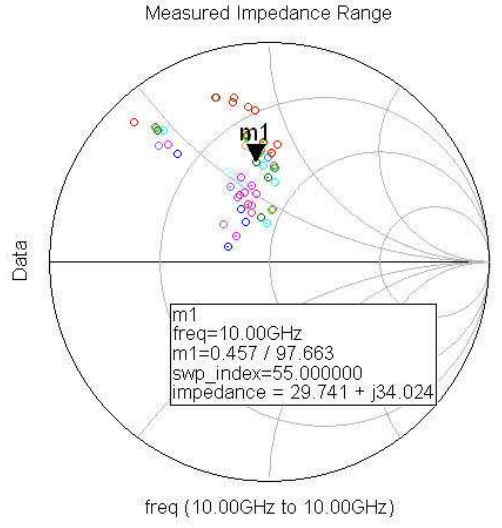
measured real part from 3.7 to 45.8 Ω, and the imaginary part from 5 to 44 Ω. The measured impedance range also shows a shrinkage compared to that of the simulated results, which indicates more loss obtained from the measurements than from the simulations.

Figure 91 shows the insertion loss comparison between the simulations and the on-wafer measurements with respects to each of the 64 different states.

Figure 91(a) shows the simulated insertion loss with the improved tuner design, which varies from 0.6 dB to 2 dB. With one single state when all the MEMS switches are at the off-state, the tuner has the most significant loss, which is 2 dB. Also noted in Figure 91(a), the switches at the upper 3 sub-circuits (Sw3, Sw2, Sw1) are dominant for the lower insertion loss. As long as one of the three switches (Sw3, Sw2, Sw1) is actuated, the tuner loss is reduced from 2 dB to 0.8 dB, from the initial state "000 000" to the next state "000 001" (state 1 to state 2 as indicated by the state address in the x-axis). After the initial state, with all the switches at the off-state, the next higher loss state is the starting state of the second group, as "001 000" (Sw4 is at the on-state), which has an insertion loss of 1.4 dB. Then, as long as one of the switches at the upper sub-circuits (Sw3, Sw2, Sw1) is at the on-state, the insertion loss reduced to be around 0.6 dB. This patterns keeps going till the last group of 8 states ("111 xxx", where 'x' stands for '1' or '0' for Sw3, Sw2, and Sw1). This indicates that the locations of the MEMS switches "Sw4", "Sw5", and "Sw6" have greater effects on the tuner insertion loss, than that of the switches "Sw1", "Sw2",

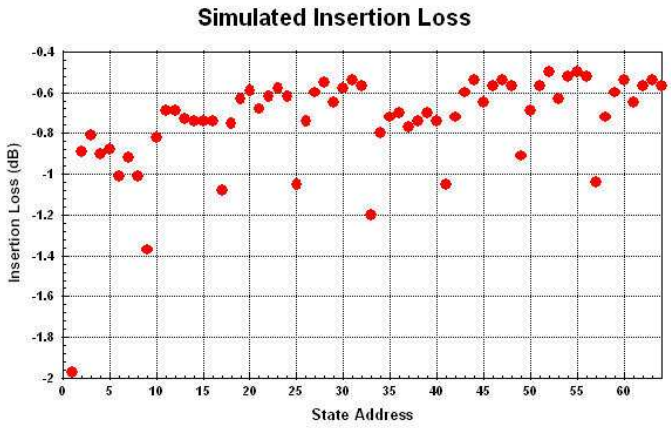



(a)

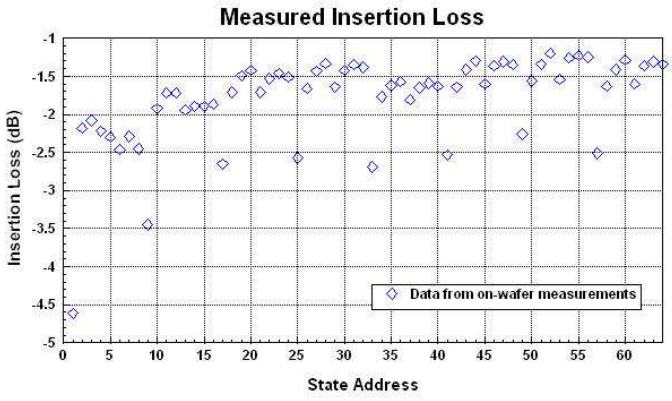



(b)

**Figure 90:** The comparison of the simulated and measured impedance range of (a) the simulated results of the tuner with the improved design (b) the measured results from the on-wafer measurement of a tuner with the improved design




(a)




(b)

**Figure 91:** The comparison of the simulated and measured insertion loss of (a) the simulated results of the tuner with the improved design (b) the measured results from the on-wafer measurement of a tuner with the improved design

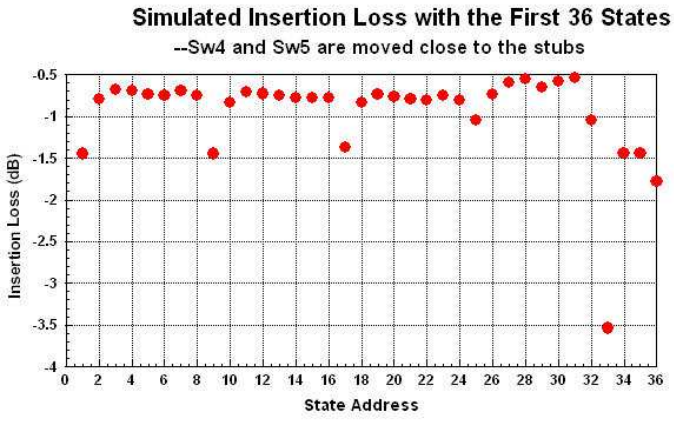



**Figure 92:** The simulated insertion loss of a tuner with the improved design when Sw4 and Sw5 are moved to be close to the radial stubs

and "Sw3". Some simulations were done to verify this analysis, and it was found that when "Sw4", "Sw5", or both of them are moved to be as close as possible to the radial stubs that they are connected to, the insertion loss at state 1 (000 000) will be improved to around 1 dB. But, the insertion loss at some other states (for example, 100 xxx, 'x' stands for '0' or '1') will increase. Similar to this, when all three switches at the lower path (Sw6, Sw5, Sw4) are moved at the same time to be close to the radial stub, the insertion loss at the initial state (000 000) gets worse to about 5 dB.

As an example, the insertion loss of the tuner when both Sw4 and Sw5 are moved close to the radial stubs are studied for the first 36 states, and the results are shown in Figure 92. It should be pointed out here that the impedances are also changed due to the different positions of the switches, but only the insertion loss is studied.

Figure 92 shows that after Sw4 and Sw5 are moved to be as close as possible to the radial stubs they are connected to, the insertion loss of the initial state (000 000) has been lowered to about 1.4 dB, as well as the insertion loss of the rest of the states in the same group maintains about the same. But starting from the 5th group of the states (Sw6 is actuated as 100 xxx, where 'x' is for '0' or '1'), the insertion loss gets worse and increased to 3.5 dB for the first state in the group. This shows that when the positions of the switches change, the tuner insertion loss for some states will be improved, but for some other states, it will increase.

This study implies that the impedance tuner with multiple MEMS switches potentially has a higher insertion loss at certain states, and the optimum value may be achieved by carefully positioning each of the switches. The goal of achieving the optimum values of the insertion loss for all the states, as well as maintaining the impedances in the required range can be challenging.

Figure 91(b) shows the measured insertion loss from the on-wafer measurements. The insertion loss at all 64 states shows the same trend as that from the simulations. But for each of the states, the insertion loss is about 1.2 to 1.5 dB higher than that from the simulated results.

The reason that causes the discrepancy of the insertion loss between the simulations and the measurements has been studied. Since this is an on-wafer measurement with TRL calibration, the calibration and measurement errors have been mostly minimized. The backside ground plane and thickness of the metal layers of the tuner has also been verified, to make sure there is enough gold for the skin depth effect. The silicon substrate and the $Si_3N_4$ have been proven to meet the specifications, ie. silicon has a high resistivity and $Si_3N_4$ is insulating, these two can be eliminated from contributing to the tuner loss.

Since the simulations and measurements for the reconfigurable bandstop filters have shown a very good agreement when all the MEMS switches are at the off-state, the fabrication processes between these two circuits were compared. The difference between them is that the highly resistive material ITO and AZO are used for the DC bias lines in the tuner development.

It is highly suspected that the highly resistive materials (ITO or AZO) was not completely etched. In order to prove this idea, some measurements were done to obtain some useful data. First, an Energy Dispersive X-Ray Spectrometer (EDX) was used with the assistance of nGimat, in the effort of spotting the location for those areas that were suspected not being etched completely, but this was not successful because of the limited number of positions of scanning. Second, when performing the DC measurement of the MEMS switches, between the input transmission line and the output transmission line of the switch, it was found some of the MEMS switches have a DC resistance even when they

are at the off-state. The DC testing shows the resistance varies from 350 KΩ to 400 KΩ. This is not to be expected, since when the membrane is at the up position, the input transmission line and the output transmission line are not connected, thus, it should show an open circuit for DC measurement. One possible reason for this could be that there is some non-uniform conductive material underneath the microstrip lines, which maybe formed by the residue of the ITO or AZO from incomplete etching. With this conductive material underneath the microstrip impedance tuner, RF energy will leak through the substrate to the ground plane, resulting in a higher loss.

There are two ways to resolve this problem for future RF circuit design with the highly resistive material as part of the DC bias lines.

First, dilute the acid used to etch these two materials to a much lower concentration. The current concentration used was 1%, it can be diluted to 0.1% to 0.5% for the future fabrication, to make sure it will be slowly etched over a long period of time. But this is not the best option, since the residue of those materials might still persist on the wafer.

Second, a different method for the highly resistive material patterning has to be used, such as lift-off, instead of chemical wet etching. This will ensure that only the patterned areas will have the resistive materials, thus, the risk of having the residue on the wafer will be eliminated.

#### *5.6.5.3 Assembled Individual Tuner Measurement and Results*

The diced individual tuner was assembled to two TMM6 boards with the 50 Ω transmission line, to measure the impedance range and the insertion loss.

The selected states of the assembled individual tuner were measured and results were compared with the simulations. The measured impedance range at 10 GHz is shown in Figure 93(a), and the measured insertion loss at the correspondent states at 10 GHz is shown in 93(b). Figure 93 shows that the impedance range for the selected states has shrunk, and the measured insertion loss of the assembled individual tuner is similar to that of the tuner from the on-wafer measurements for the selected states.

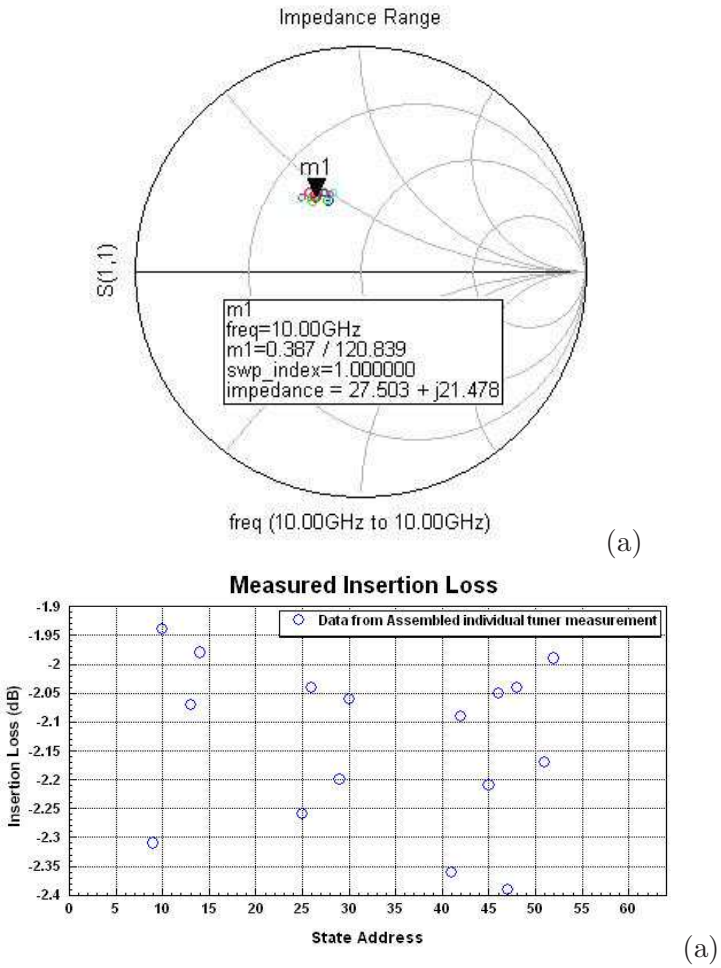



**Figure 93:** The measured results from the selected states of an assembled individual tuner of (a) the impedance range at 10 GHz (b) the insertion loss at 10 GHz

## *5.7 Conclusions*

A monolithic impedance tuner on a high resistivity silicon wafer has been designed to provide the tunable output matching network for high efficiency power amplifiers. The simulated and the measured results show a good agreement. The simulated impedance range is 3.2 to 57.5 Ω for the real part, and -2.4 to 55.2 Ω for the imaginary part; the measured impedance range is 3.7 to 45.8 Ω for the real part, and 5 to 44 Ω for the imaginary part. The tuner insertion loss was fully characterized and compared to the simulated results. The insertion loss from the on-wafer measurements at the nominal impedance is 1.2 dB, with an average loss of about 1.5 dB at all total of 64 different states. The max incident power has been

measured to be 1 Watt, with a measured S(1,1) = 0.5076/94.69° of the tuner at the nominal impedance state (state 55 as shown in Figure 90), the input power delivered to the tuner is $P_{inc} \times (1 - |S(1,1)|^2) = 1$ watt $\times$ 0.742 = 742 mW = 28.7 dBm. In other words, the tuner has been measured to sustain a 28.7 dBm of RF power.

To the author's knowledge, this is the first reported reconfigurable impedance tuner using RF MEMS switches that has been thoroughly characterized on the tuner RF performance, including both the impedance range and the insertion loss.

# CHAPTER VI

# RECONFIGURABLE SELF-SIMILAR FRACTAL ANTENNA USING RF MEMS SWITCHES

Reconfigurability in an antenna system is a much-desired characteristic that has been the focus of much research in recent years [16,27,51]. In this project, cantilever DC contact RF-MEMS switches are integrated with self-similar planar antennas to provide a reconfigurable antenna system that radiates with similar patterns over a wide range of frequencies. The single antenna part was designed at the University of New Mexico [21]. The challenge comes from the integration of the MEMS switches to the antenna, DC bias lines implementation, and an efficient layout generation toward a successful fabrication of the antenna. The antenna s-parameters testing was done at Georgia Tech with VNA. The radiation pattern was taken at NASA Glenn Research Center. Measured results were compared with the simulations, the data is analyzed and future improvement for integrated antenna design is proposed.

## *6.1 Design Review*

### 6.1.1 Background

Reconfigurable RF-MEMS antenna systems were first introduced in 1998 by E. R. Brown [51] and since then have been studied by several research groups. An emphasis has been given in reconfigurable aperture (recap) and microstrip antenna structures, in order to achieve multiple octave tunability [16, 27, 51, 52]. Still, the integration of RF-MEMS with the antenna has not been fully demonstrated. In the majority of the publications, ideal models for the switches were used. Also, the effect of the bias lines on the antenna has been largely neglected.

The distributions of the currents on the surface of an antenna are inherently related to its radiation patterns. Predetermining these current paths, allows us to define the antenna's

radiation patterns in the various frequencies of operation. The feature of self-similarity of a fractal antenna provides the basis for the design of multiple-frequency antennas. These antennas have the advantage of radiation with similar patterns in a variety of frequency bands. The major predecessor is the widely studied Sierpinski Gasket [53, 54]. In an ideal case, the Sierpinski Gasket is described by an infinite number of iterations resulting in a very complex antenna structure with an infinite number of frequency bands. In reality though, technological limitations reduce the number of iterations for such a structure to less than 6 (pre-fractal). In [21], 2 iterations were used to obtain the desired reconfigurability. Reference [21] introduced and discussed an analytical procedure used to design the antenna, and the main idea is to demonstrate the function of a new type of RF-MEMS reconfigurable multiband antenna based on a fractal design.

The original antenna design provided by the University of New Mexico was two separate antennas with one triangle at each side of the citation for the resonant frequency at 14 GHz, and another one with three triangles on each side of the citation for the resonant frequencies at 8 and 25 GHz. The idea of tunability was realized by adding a perfect open or a perfect short between the first triangle and the second two triangles. This perfect open or short was used to model the MEMS switch when it's at the off- or on-state.

The DC contact MEMS switches was used for the reconfigurability of the antenna. The detailed MEMS switch model was provided and they are used to replace the perfect short and open in the original design. The layout of the antenna with the integration of MEMS switches is shown in Figure 94.

The operation of the antenna is as follows: the reconfigurable antenna may contain both similar and dissimilar radiating (or receiving) elements. Using these switches (totally four as in Figure 94), a bowtie mode of operation (all switches 'off') and a MEMS-enabled (or fractal) mode of operation (all switches 'on') can be obtained. Since the 'fractal' mode's active structure consists of two iterations, we anticipate two different resonant frequencies. Two more non-symmetric configurations can also be obtained with one switch 'on' and one 'off' on each arm. The result is a total of 4 different paths for the currents to flow and hence 4 possible antenna configurations to be used. As previously mentioned, the self-similarity

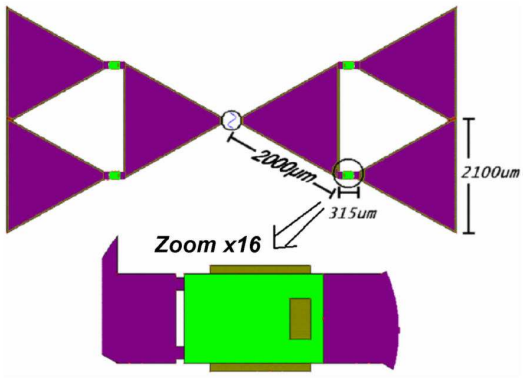


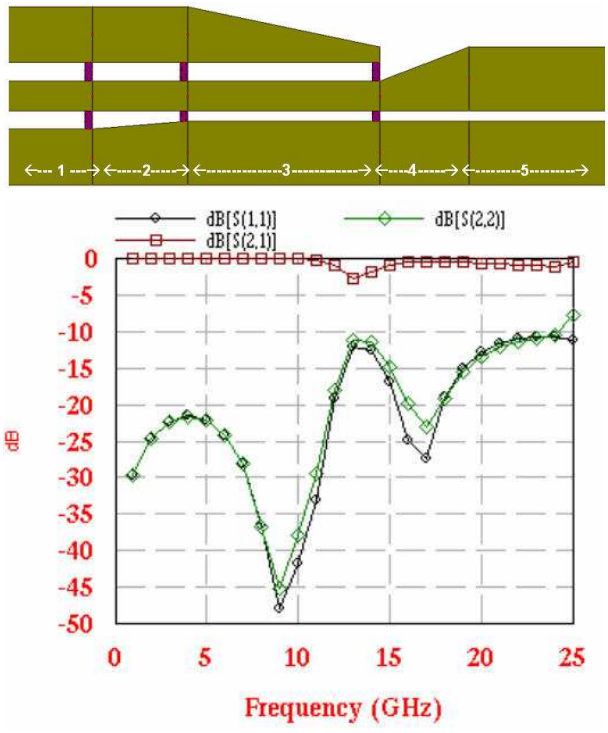

**Figure 94:** The design layout of the reconfigurable fractal antenna with DC contact RF MEMS switches

between the 2 major modes ('bowtie' and 'fractal') results in similar radiation patterns. The two non-symmetric modes were only simulated but exhibited patterns similar to the planar dipole as well. The initial antenna dimensions and the switch placement are shown in Figure 94. Proper function and connection of the electrostatic actuators imposes many structural restrictions on the antenna's materials and especially on its substrate layers, which requires a very consistent fabrication process, and thus the final layout of integration of the antenna to MEMS switches has to be carefully considered.

Several antenna designs achieve the desired performance. The criteria used to pick the final design are both performance and bandwidth for a particular bow-angle, over the antenna's operational frequencies. Our initial goal was to design a reconfigurable multiband antenna that resonates primarily at 14 GHz, and that can resonate on-demand, at two more frequency bands, preferably around 8 GHz and 25 GHz. Almost all the tested antennas exhibited radiation patterns similar to that of a planar dipole, at their respective resonances.

Since the antenna is in CPS (Coplanar Stripline) configuration, and most of the RF probes are in CPW (Coplanar Waveguide) configuration for the on-wafer measurement, a transition from CPW to CPS was designed [21] for the antenna feedline. The feedline was chosen to be 4 mm long to be far away from antenna radiating body. The picture of the transition and the transition response are shown in Figure 95 (a) and (b) [21].

Figure 95 (a) shows the layout for the transition from CPW to CPS. The center signal line width of the CPW line is 47 $\mu$m, the width of the group strips is 171 $\mu$m, the gap




(a)

(b)

**Figure 95:** The transition from CPW to CPS for the antenna feedline. (a) The transition layout (b) The transition response

between the center line and two group strips is 20 $\mu$m. This requires using RF probe with a pitch of 150 $\mu$m for the on-wafer measurements.

Figure 95 (b) shows the simulated frequency response of the CPW to CPS transition. It shows that the return loss is less than -10 dB from 1 to 25 GHz, and the insertion loss is less than 1 dB, while it has a small resonance around 13 GHz, this might result in a resonance in the antenna measurement at this frequency.

To simplify the fabrication, the air bridges in Figure 95 are not fabricated. Instead, wire bonds are used to connect the ground strips of the CPW feedline. Due to a tight space in this area, it's very hard to control the height and the shape of the wire, thus, the inductance effect of the wire can only be approximated. Hence, the antenna performance has slightly altered in the measured results from the simulated results.

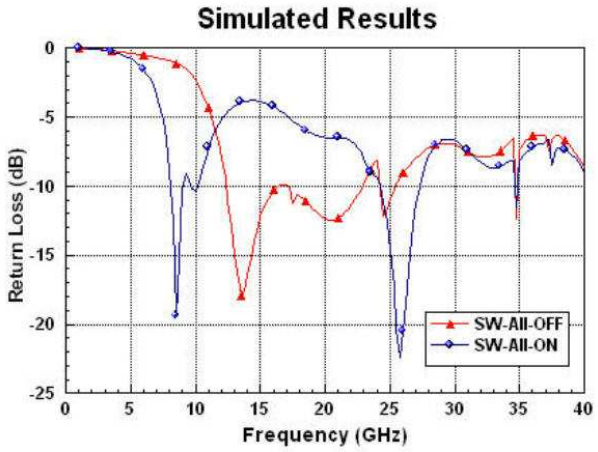



**Figure 96:** The simulated antenna return loss with MEMS switches at both off- and on-state

### 6.1.2 Simulated Results

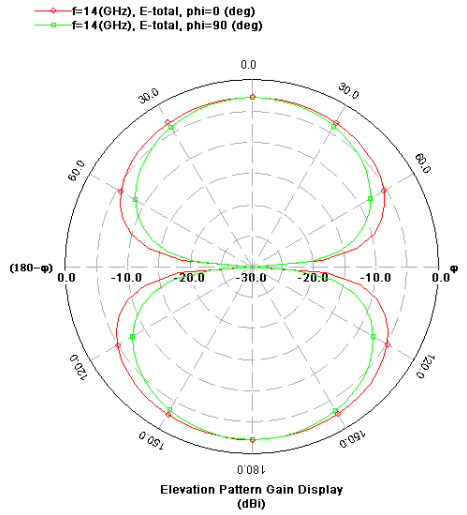
The simulated antenna resonates at three frequencies with a return loss higher than 15 dB. These are: $f_1$ (sierp 1) = 8 GHz, $f_2$(bowtie) = 13.5 GHz, and $f_3$(sierp 2) = 25.75 GHz with respective bandwidths: $Bw_1 = 1$ GHz, $Bw_2 = 4$ GHz and $Bw_3 = 3$ GHz. The bowtie mode is also fairly well matched from 17 GHz to 22.5 GHz exhibiting the same radiation pattern as at 14 GHz. This resonance comes from the feedline, and even though its pattern is also dipole-like, the use of it solely depends on the performance of the measured model.

The simulated return loss is shown in Figure 96. As it can be seen, when all the MEMS switches are at the off-state, the antenna has a resonant frequency at about 14 GHz and it's a wide band matching; when all the switches are at on-state, it has two resonant frequencies at 8 GHz and 25 GHz.

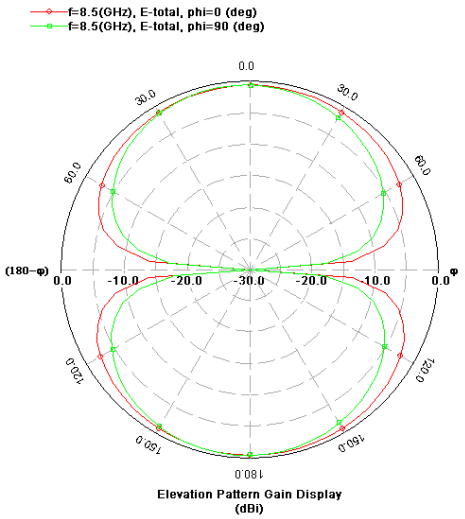
Figure 97 shows the reconfigurable antenna radiation pattern at different resonant frequencies.

The simulated antenna radiation pattern include both of the results and without the DC bias lines. The highly resistive material used for the DC bias lines is AZO as it has shown a good performance from impedance tuner. The design for the DC bias line is described in the next section.

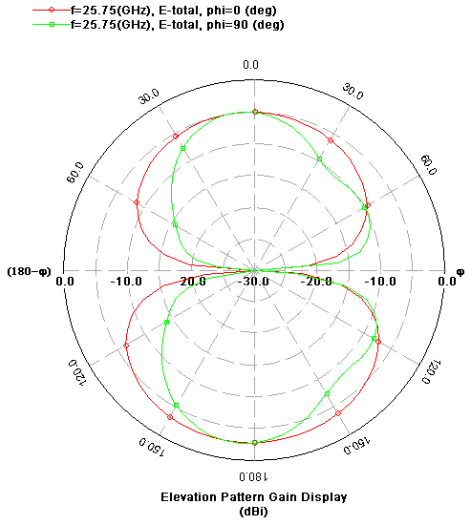
In Figure 97, it can be seen that the antenna with different states (off- or on-state) of




(a)




(b)




(c)

**Figure 97:** The simulated antenna radiation pattern (a) at 14 GHz when all the DC contact MEMS switches are at off-state (b) at 8 GHz when all the DC contact MEMS switches are at on-state (c) at 25 GHz when all the DC contact MEMS switches are at on- state

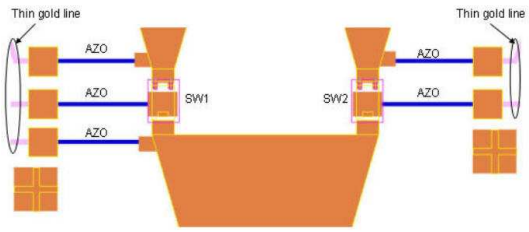



**Figure 98:** The partial picture of the antenna with MEMS switches and DC bias lines

the MEMS switches radiates in the broadside direction, with patterns very similar to each other. The 25.75 GHz simulated pattern is slightly deformed towards the $\phi = 90°$, most probably due to the long feed structure. And, the antenna's directivity is maximum towards the dielectric side at all frequencies.

## *6.2 DC Bias Line Implementation and Layout Design*

As the MEMS switches are integrated with the antenna, the DC bias lines must be designed properly, in order to actuate the MEMS switches as well as not to degrade the antenna performance, in terms of both return loss and radiation patterns. And, prior to fabrication, a very inclusive layout has to be generated.

### 6.2.1 DC Bias Line Implementation

The DC bias lines consist of two materials as mentioned earlier, which is the highly resistive material and the thin layer of gold lines. For the tunable antenna, the resistive material used is AZO (Aluminum doped Zinc Oxide) which is deposited on silicon wafers coated with 1 $\mu$m of $SiO_2$. The deposition of AZO was done with the assistant of nGimat, by using CCVD with chamber temperature at 350°C. In the DC bias lines, the highly resistive AZO was placed as close as possible to the antenna triangle part but not underneath it, in order to avoid any additional loss from this material. The configuration of DC bias lines close to the antenna part is shown in Figure 98.

As it is shown in Figure 98, the DC bias lines for the MEMS switches are composed of two types of materials: the blue lines in the picture are highly resistive material AZO; the pink lines in the picture are thin layer of gold lines patterned with lift-off process which are

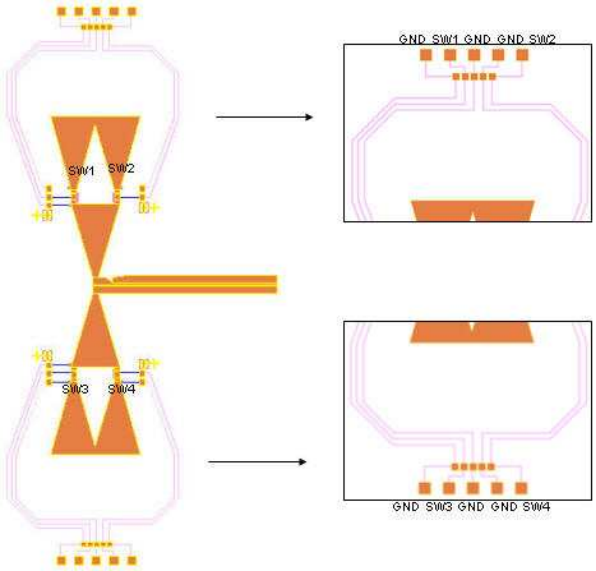



**Figure 99:** The reconfigurable antenna layout with the RF MEMS switches and the DC bias lines

in direct contact with AZO and the DC probe pads. The thickness of the AZO is about 300 $\AA$, and its sheet resistance is about 200 KΩ/square to 500 KΩ/square, which is very non-uniform. And, on the edge of the wafer, the sheet resistance is much higher than that in the center of the wafer. In order to achieve a high DC resistance for the DC bias lines, the width of the AZO is designed to be 25 $\mu$m while the length is 500 $\mu$m, which is equivalently 20 squares. Theoretically this will give about 4 MΩ and above for the DC resistance, which is sufficient to block the RF energy leakage through DC paths.

The thin gold lines connecting to the AZO lines are then brought close together and connected to five DC probe pads, which consist of 3 grounds and 2 voltages (as GSGSG-type) and have dual pitch (150 $\mu$m and 400 $\mu$m) in order to be able to use for any available DC probe cards. Since the DC pads have only 3 grounds, the third one is used as a common DC ground for both of the MEMS switches in the same group. The final single antenna layout is as shown in Figure 99.

Figure 99 shows the reconfigurable antenna layout with the DC bias lines, and the close-up for DC bias lines with the layout for the DC probe pads. For each group of DC probe pads, it has two sets of DC pads: the first one has a smaller pitch which is 150 $\mu$m; the second one has a pitch of 400 $\mu$m. The distance from the DC probe pads to the edge of

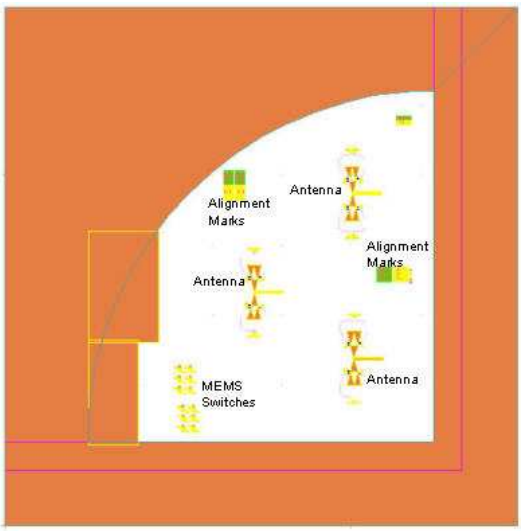



**Figure 100:** The final mask layout for antenna fabrication

the antenna is 2.5 mm. As is shown later from the measurements, a longer distance needed to be used to avoid energy reflection from DC probe tips. All DC bias lines are fabricated underneath the thin layer of $Si_3N_4$ in order to protect them from future fabrication process.

### 6.2.2 Fabrication Layout generation

After the single antenna layout is done, a complete mask layout has to be generated for the fabrication purpose. As shown previously, the fabrication is done on a quarter piece of 4" wafers, thus it has limited space. To avoid each antenna interacting with others, the best scenario is to just place one antenna on each wafer. But this will increase the risk of no functioning antenna when there is a yield issue. Considering this, 3 antennas were placed on different locations on the same wafer with around 20 mm apart, which is proved sufficient enough to avoid the cross talk among the antennas. The final mask layout is shown in Figure 100, which is a multi-layered mask file.

As shown in Figure 100, three antennas are fabricated at one time on the same wafer. What is also included in the antenna mask layout is the discrete DC contact MEMS switches, which are fabricated on the same wafer in order to characterize the MEMS switch performance.

Since the reconfigurable antenna used the DC contact MEMS switches, it has the same

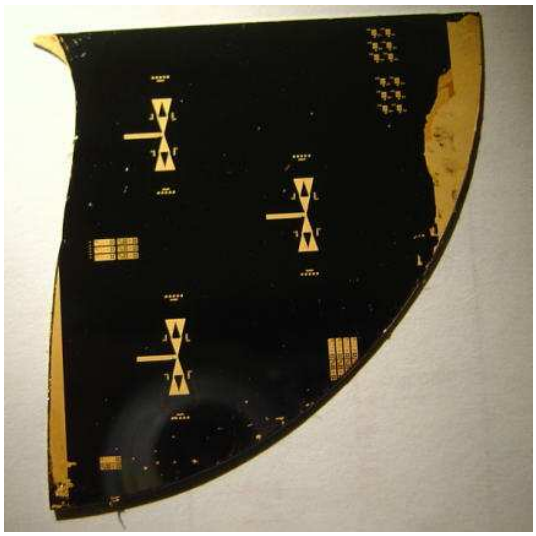


**Figure 101:** The fabricated circuits on a quarter piece of a 4" wafer

fabrication process as for reconfigurable impedance tuner. The detailed fabrication process is included in Appendix III. The picture of a fabricated circuit is shown in Figure 101.

## *6.3 Measurements and Results*

The measurements of the antenna system include the s-parameter measurement to obtain the return loss, and the radiation pattern measurement.

When performing the measurement, a 1 cm thick foam spacer was used underneath the Si wafer to keep the antenna away from the probe station made of aluminum. The reason for this is that the antenna on the silicon wafer is in CPS configuration, however, if it is placed immediately on the probe station, a different mode will be excited as well as the energy will radiate through the substrate to the ground plane provided by the metal probe station. This will alter the antenna performance. The foam spacer used has a relative permittivity of 1.0001 which is very close to that of the air. Thus, it won't have any effects to the antenna performance.

### 6.3.1 S-Parameter measurement

The s-parameter measurement was done by using an Agilent 8510C network analyzer and a Cascade probe station. A GGB industries RF probe with a pitch of 150 $\mu$m was used for the on-wafer probing, a DC bias Tee was connected between the VNA and the RF cable

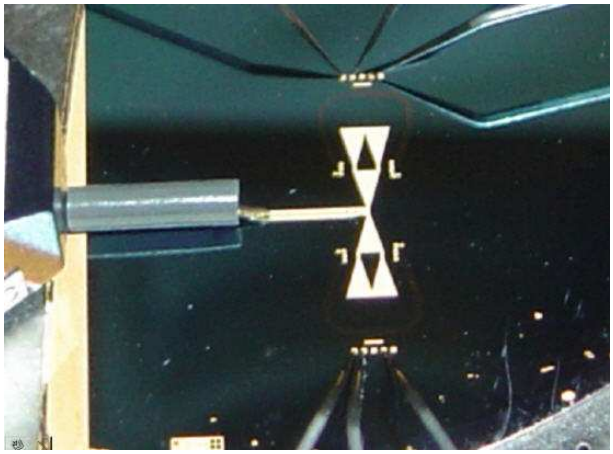


**Figure 102:** The picture of a fabricated reconfigurable antenna in the measurement

to provide the common DC ground, and 6 other DC probes were used for the DC voltage application.

Since the antenna is a one port network, the calibration is relatively easy. The calibration method used is SOLT with short-open-load, and the reference plane was calibrated so it is at the end of the CPW feedline. A DC bias Tee was first connected to the vector network analyzer to provide the DC ground through the RF path. Figure 102 shows the picture of the antenna in the middle of the measurement.

With this setup, the common DC ground is provided through the DC bias Tee and connected to the center signal line of the CPW feed line. The other 6 DC probes, instead of probe cards, are used to provide the DC voltage to the bottom electrode, and the bottom contact metal of the DC contact MEMS switches.

The comparison between the antenna's simulated and measured return loss is shown in Figures 103 and 104. It is evident that the antenna's performance changes when the DC probes are nearby or away from it, regardless of the applied voltage. This is due to the metallic tips creating reflections of the radiated energy and deteriorating the antenna's performance.

The antenna is first measured when all the MEMS switches are at off-state; the measured results compared to the simulated results are shown in Figure 103. As it can be seen, there are two situations from the measurements: 1) All the DC probes are placed away from the

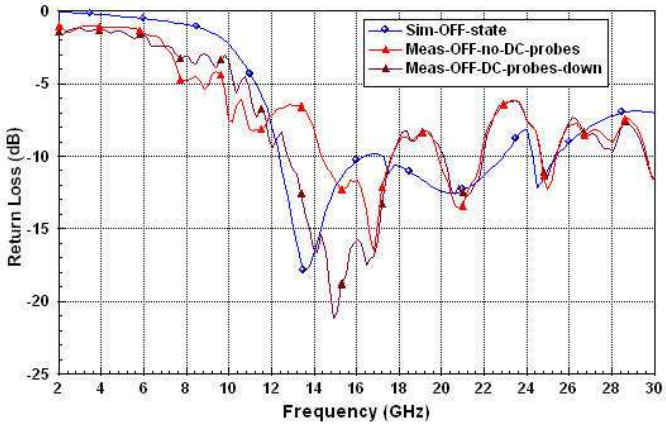



**Figure 103:** The comparison of the simulated and measured return loss when all the MEMS switches are at the off-state

DC probe pads, a resonance at 16.5 GHz is measured. Its bandwidth is from 14.2 GHz up to 17.5 GHz. A weak resonance is also noticed at 21 GHz, due to the antenna feedline as mentioned previously. 2) All the DC probes are brought down and in contact with the DC pads without the DC voltage application, the antenna resonates at 15 GHz, with a bandwidth from 12.75 GHz up to 17.5 GHz, and covers the desired band at 14 GHz. Since the antenna will be constantly changing configuration, it is energy efficient to keep the probes connected to the antenna.

Then, the antenna is measured when all the MEMS switches are at the on-state; the comparison between the measured results and the simulated results is shown in Figure 104. As it can be seen, the antenna resonates at two frequencies, very close to the simulated ones. The first one occurs at 9.2 GHz, with a bandwidth of 1.6 GHz; and the second one is at 25.2 GHz, with a bandwidth from 24.3 GHz up to 28.2 GHz. The antenna maintains a good match up to 32.2 GHz. Again, there is a very weak resonance at 21.5 GHz, due to the antenna feed line. The overall measured performance of the antenna showed some minor frequency shifts compared to the simulations.

### 6.3.2 Radiation Pattern Measurement

The radiation pattern measurement was done at NASA Glenn research center, and follows the procedure outlined below [21]:

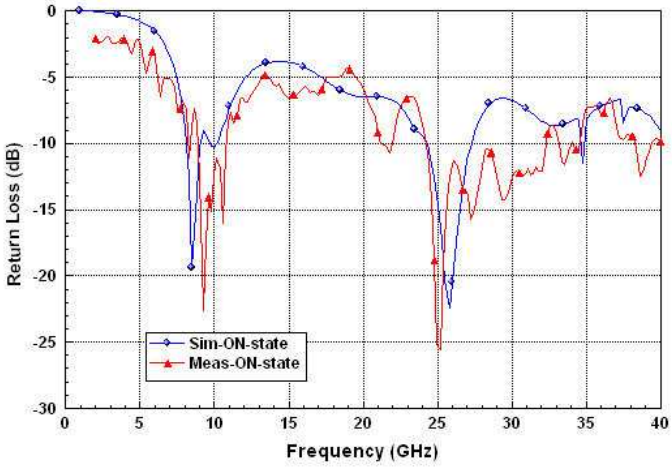



**Figure 104:** The comparison of the simulated and measured return loss when all the MEMS switches are at the on-state

The antenna radiation pattern is measured in a unique, far field antenna range that is designed for measuring antennas while they are on an RF probe station. The antenna under test is the transmitting antenna and is fed by a ground-signal-ground RF probe, while the receiving antenna is a half wavelength dipole that is fed by a coaxial cable. The RF signal is modulated by a 20 MHz signal, which is detected by a diode detector and measured by a lock-in amplifier. The receiving dipole antenna is rotated around the antenna under test, with the distance between the two antennas fixed at 9 cm. To bias the MEMS switches, two five-pin DC probes card with a pitch of 150 $\mu$m are used, with one on each side of the antenna under test. Because the antenna under test radiates uniformly in the theta direction, the Si substrate is placed on 1 cm of absorbing material to minimize effects of the metal wafer chuck. Furthermore, absorbing material is judiciously placed around the antenna under test to minimize the effects of the RF and DC probes, the coaxial dipole and the plexiglass rod that holds it, and the RF probe station. Because the probes and the absorbing material interfere with the measurement system, the data is only plotted over the range where the two antennas are in view of each other. Even with these precautions, there is still ripple in the measured radiation pattern due to the reflecting surfaces. The measured and simulated radiation patterns are shown in Figures 105 to 107. Even though the measured results show some ripple, similarity with the expected simulated patterns is

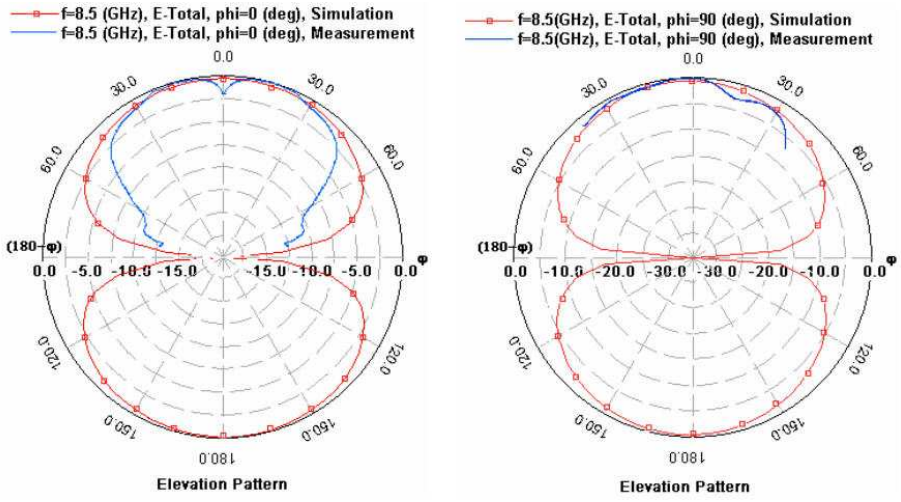



**Figure 105:** The comparison of the simulated and measured radiation pattern at 8 GHz of the reconfigurable antenna when all the MEMS switches are at the on-state

evident. The reason that the measurements show a lower magnitude towards the broadside direction is that there is a thin piece of absorber on the wafer, and this partly absorbs some of the power at this angle. This absorber had to be added to eliminate radiation from sections of Au on the wafer that were causing severe ripple in the patterns.

## *6.4 Conclusions*

A reconfigurable multiple-frequency fractal antenna system was integrated, fabricated and tested. The antenna radiates in three frequency bands with similar radiation patterns. This system is, to the best of our knowledge, the first functional fully integrated RF-MEMS reconfigurable fractal antenna. The complete system was simulated and measured and the obtained results were presented in this chapter.

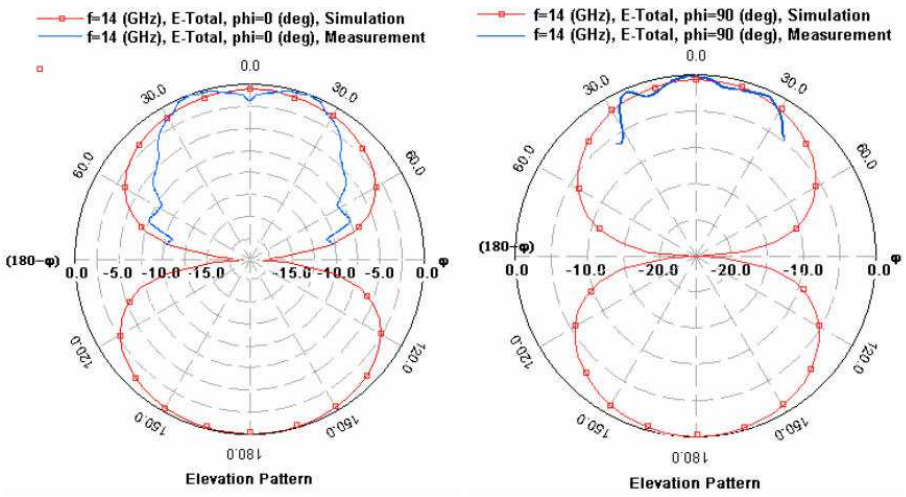



**Figure 106:** The comparison of the simulated and measured radiation pattern at 14 GHz of the reconfigurable antenna when all the MEMS switches are at the off-state

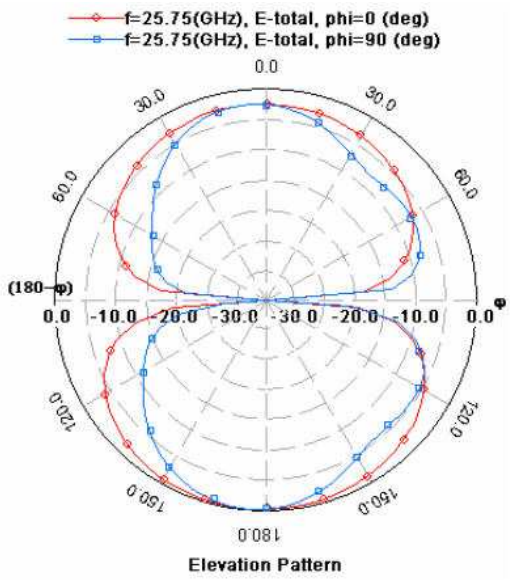



**Figure 107:** The comparison of the simulated and measured radiation pattern at 25 GHz of the reconfigurable antenna when all the MEMS switches are at the on-state

# APPENDIX A

# FABRICATION PROCESS RECIPE FOR THE CPW RF PROBE PAD TO MICROSTRIP TRANSITIONS – (SINGLE METAL LAYER FABRICATION PROCESS)

## *A.1 Wafer Preparation*

### A.1.1 Wafer Dicing

Use diamond pen to dice a full 4" wafer into 4 pieces.

### A.1.2 Clean

Soak the wafer in Actone and then IPA (Isopropyl Alcohol) for 5 minutes with each solvent, respectively.

### A.1.3 Dry

Blow dry the wafer with Nitrogen gun, and soft bake for 2 min on a hotplate preset temperature at 120°C.

## *A.2 $SiO_2$ Deposition*

Use STS or Unaxis PECVD to deposit 1 $\mu$m of $SiO_2$ on top of the silicon wafer.

### A.2.1 Deposit $SiO_2$ with STS PECVD

#### *A.2.1.1 Run Clean Process*

Run clean process for 2 hours, using recipe: clean.set.

#### *A.2.1.2 Run Deposition Process*

Deposit $SiO_2$ for 15 min to a thickness of 1 $\mu$m, using recipe: lfsin.set

### A.2.2 Deposit $SiO_2$ with Unaxis PECVD

#### *A.2.2.1 Run Clean Process*

Run clean process for 2 hours, using recipe: clean_250.set. This makes sure the clean process is done at 250°.

#### *A.2.2.2 Run Deposition Process*

Deposit $SiO_2$ for 25 to a thickness of 1 $\mu$m, using recipe: EM_sin.set. The deposition is done at 250°C.

## *A.3 Seed Layer Deposition*

This is done for both sides of the wafer.

### A.3.1 Deposit Ti/Au/Ti

Use E-beam evaporator to deposit Ti/Au/Ti for a thickness of 300/2500/200 $\mathring{A}$, with the deposition rate of 2 $\mathring{A}$/sec for each material. The deposition starts when the vacuum is at 2.0 x $10^{-6}$ Torr or lower.

## *A.4 Backside Ground Plane Electro-Plating*

### A.4.1 Protect the front side with Shipley SC1827

#### *A.4.1.1 Spin*

Spin Shipley SC1827 on the front side of the wafer with the spinning speed of: starting at 1000 rpm, with a ramping speed of 300 rm for 5 sec; and spinning 3000 rpm, with a ramping speed of 700 rm for 30 sec.

#### *A.4.1.2 Bake*

Bake the wafer on a hotplate with the temperature preset at 120°C for 1.5 min.

### A.4.2 Etch Ti layer

#### *A.4.2.1 Dilute HF*

Dilute HF with DI water to a concentration of HF:$H_2$O as 1:10.

#### *A.4.2.2 Etch Ti*

Use tweezer to hold the wafer and dip it into the HF solution to etch Ti, for 4 to 6 sec. Slightly agitate.

#### *A.4.2.3 Clean*

Rinse with DI water thoroughly and blow dry.

### A.4.3 Setup Gold-plating station

#### *A.4.3.1 Connect the Wires for the Plating Station*

Two Teflon boards are used: one has the metal mesh on it to connect to the cathode, and other one has a metal clip attached to the board with a small tip which is used to be in contact with the wafer, which will be connected to the anode. These two boards are placed inside the bottle with the gold solution.

#### *A.4.3.2 Setup Plating Station Parameters*

The output current of the DC source is set at 10 mA; the probe temperature is at 55°C and the stirrer spinning speed is at 200 rpm.

### A.4.4 Electro-Plate Gold

Wait for the solution temperature stable at 55°.

#### *A.4.4.1 Connect the Wafer*

Clip the wafer onto the board that connects to the anode, make sure there is a good DC contact.

#### *A.4.4.2 Electro Plate the gold*

Plate for 35 min.

#### *A.4.4.3 Clean*

Rinse with DI water, and blow dry.

### A.4.5 Remove Photoresist on the Frontside

#### *A.4.5.1 Clean*

Clean wafer with Acetone and IPA, blow dry.

#### *A.4.5.2 Bake*

Bake wafer on a hotplate at 120°C for 2 min.

## *A.5 Protect the Backside Using Shipley SC1827*

### A.5.1 Spin

Spin Shipley SC1827 on the backside of the wafer with the following spinning speed: starting at 1000 rpm, with a ramping speed of 300 rm for 5 sec; and spinning as 3000 rpm, with a ramping speed of 700 rm for 30 sec.

### A.5.2 Bake

Bake the wafer on a hotplate preset at 120°C for 1.5 min.

## *A.6 Electro-Plate the Front Side (Clear Field Mask)*

### A.6.1 Pattern the Front Side with Shipley SC1827

#### *A.6.1.1 Spin*

Spin Shipley SC1827 with the spinning speed: starting at 1000 rpm,with a ramping speed of 300 rm for 5 sec; and spinning at 3000 rpm, with a ramping speed of 700 rm for 40 sec.

#### *A.6.1.2 Bake*

Bake the wafer on a hotplate with the temperature preset at 120°C for 20 min.

#### *A.6.1.3 Expose*

Use right MJB-3 channel 1 with intensity of 3 mW/$cm^2$, expose for 55 sec.

#### *A.6.1.4 Develop*

Use tweezer to hold the wafer and dip it into the Microposit 354 developer for 20 to 22 sec, slightly agitate.

#### *A.6.1.5 Clean*

Rinse with DI water, blow dry.

#### *A.6.1.6 Inspection*

Check features with microscope; then check thickness with alpha-step profolometer, which is about 3 $\mu$m thick.

### A.6.2 Etch Ti layer

#### *A.6.2.1 Dilute HF*

Dilute HF with DI water to a concentration of HF:$H_2$O as 1:10

#### *A.6.2.2 Etch Ti*

Use tweezer to hold the wafer and dip it into the diluted HF, to etch Ti for 4 to 6 sec.

#### *A.6.2.3 Clean*

Rinse with DI water thoroughly and blow dry.

### A.6.3 Setup Gold-plating station

#### *A.6.3.1 Connect the Wires for the Plating Station*

Use the same setup as above.

#### *A.6.3.2 Setup Plating Station Parameters*

The output current of the DC source is set at 7.8 mA; the probe temperature is at 55°C and the stirrer spinning speed is at 200 rpm.

### A.6.4 Electro Plate Gold

#### *A.6.4.1 Connect the Wafer*

Clip the wafer onto the board that connects to the anode, make sure there is a good DC connection.

#### *A.6.4.2 Electro Plate the gold*

Plate for 30 min.

#### *A.6.4.3 clean*

Rinse with DI water, blow dry.

#### *A.6.4.4 Inspection*

Check features with microscope; then check thickness with alpha-step profolometer, make sure the plated gold is about 3 $\mu$m thick. If not, the wafer needs to be placed back to the plating station and continue with the gold plating. This step repeats until the plated thickness is about 3 $\mu$m.

### A.6.5 Remove Seed layer

#### *A.6.5.1 Remove photoresist*

Flood expose the front side of the wafer with right MJB-3 channel 1 for 1.5 min.

#### *A.6.5.2 Develop*

Develop with microposit 354 developer for 1 min.

#### *A.6.5.3 Rinse*

Rinse with DI water and blow dry.

#### *A.6.5.4 Etch Ti*

Etch Ti with HF:$H_2$O as 1:10 for 4 to 6 sec.

#### *A.6.5.5 Rinse*

Rinse with DI water thoroughly, blow dry.

#### *A.6.5.6 Etch Au*

Etch Au with gold etchant for 15 sec.

#### *A.6.5.7 Rinse*

Rinse with DI water thoroughly, blow dry.

#### *A.6.5.8 Etch Ti*

Etch Ti with HF:$H_2$O as 1:10 for 4 to 6 sec.

#### *A.6.5.9 Rinse*

Rinse with DI water thoroughly, blow dry.

#### *A.6.5.10 Clean*

Clean the wafer with Actone and IPA, to remove the photoresist on the backside of the wafer.

#### *A.6.5.11 Bake*

Bake the wafer on hotplate at 120°C for 2 min.

## *A.7 Fabrication Done*

# APPENDIX B

# FABRICATION PROCESS RECIPE FOR RECONFIGURABLE BANDSTOP FILTER - CANTILEVER CAPACITIVE MEMS SWITCH FABRICATION PROCESS

## *B.1 Wafer Preparation*

### B.1.1 Dice

Dice a 4" silicon wafer into 4 equal pieces.

### B.1.2 Clean

Soak the wafer in Actone and then IPA for 5 minutes with each solvent.

### B.1.3 Dry

Blow dry the wafer with Nitrogen gun, and soft bake for 2 min, on hotplate at 120°C.

## *B.2 $SiO_2$ Deposition*

Use STS or Unaxis PECVD to deposit 1 $\mu$m of $SiO_2$ on top of the silicon wafer.

### B.2.1 Deposit $SiO_2$ with STS PECVD

#### *B.2.1.1 Run Clean Process*

Run clean process for 2 hours, using recipe: clean.set.

#### *B.2.1.2 Run Deposition Process*

Deposit $SiO_2$ for 15 min to a thickness of 1 $\mu$m, using recipe: lfsin.set

### B.2.2 Deposit $SiO_2$ with Unaxis PECVD

#### *B.2.2.1 Run Clean Process*

Run clean process for 2 hours, using recipe: clean_250.set. This makes sure the clean process is done at 250°.

#### *B.2.2.2 Run Deposition Process*

Deposit $SiO_2$ for 25 to a thickness of 1 $\mu$m, using recipe: EM_sin.set. The deposition is done at 250°C.

## *B.3 Bottom Electrode Lift-Off (clear field mask)*

### B.3.1 Pattern with Clariant AZ5214

#### *B.3.1.1 Spin photoresist*

Spin AZ5214 on the wafer with the following parameters: starting at 1000 rpm, with a ramping speed of 300 rm for 5 sec; and spinning at 3000 rpm, with a ramping speed of 700 rm, for 30 sec.

#### *B.3.1.2 Pre-Bake*

Bake the wafer on hotplate at 110°C for 1.5 min.

#### *B.3.1.3 Expose*

Use right MjB-3 channel 1 with the intensity of 3 mW/$cm^2$, for 12 sec.

#### *B.3.1.4 Post-Bake*

Bake wafer on hotplate at 120°C for 2 min.

#### *B.3.1.5 Flood Expose*

Remove the mask from MJB-3 and flood expose the wafer for 1.5 min.

#### *B.3.1.6 Develop*

develop with Microposit 354 Developer for 20 to 22 sec; or AZ 400k: $H_2O$ as 1:4 for 20 sec.

#### *B.3.1.7 Rinse*

Rinse with DI water, blow dry.

### B.3.2 Inspection

Check features with microscope, and check the thickness with the alpha-step profolometer. The thickness is about 1.2 $\mu$m.

#### *B.3.2.1 Bake*

Bake wafer on hotplate at 120°C for 50 sec.

### B.3.3 Deposit Metal with E-Beam Evaporator

#### *B.3.3.1 Wafer Mounting*

Mount the wafer on the wafer holder and place it inside the E-beam evaporator chamber.

#### *B.3.3.2 Deposition*

Deposit Ti/Au for the thickness of 300/2000 $\mathring{A}$ starting with the vacuum at 2.0x10$^{-6}$ torr. Deposition rate is 2 $\mathring{A}$/sec for both materials.

### B.3.4 Lift-off

#### *B.3.4.1 Soak with Acetone*

Soak the wafer into a beaker with Acetone. Vibrate with ultra-sonic bath for 30 sec to 1 min, take the wafer out of the beaker, and clean the beaker with the DI water. Fill the beaker with Actone and leave the wafer in the beaker for 1 to 2 hours.

#### *B.3.4.2 Rinse*

Rinse with DI water, blow dry.

#### *B.3.4.3 Inspection*

Check features to make sure the lift-off is done successfully.

#### *B.3.4.4 Bake*

Bake the wafer at 120°C for 2 min.

## *B.4 Backside E-beam Deposition*

### B.4.1 Wafer Mounting

Mount the wafer on the wafer holder and place it inside the E-beam evaporator chamber.

### B.4.2 Deposition

Deposit Ti/Au for the thickness of 300/2000 $\mathring{A}$ starting with the vacuum at 2.0x10$^{-6}$ torr. Deposition rate is 2 $\mathring{A}$/sec for both materials.

## *B.5 $Si_3N_4$ Patterning (Dark Field Mask)*

### B.5.1 $Si_3N_4$ Deposition with Unaxis PECVD

#### *B.5.1.1 Chamber Clean*

Run clean process at 250°C, using recipe clean_250.set.

#### *B.5.1.2 Wafer Loading*

Move wafer into the chamber.

#### *B.5.1.3 $Si_3N_4$ Deposition*

Deposit $Si_3N_4$ for 35 min to a thickness of 3000 $\mathring{A}$, using recipe EM_SIN_250.set.

### B.5.2 Pattern with Shipley SC1827

#### *B.5.2.1 Spin*

Spin SC1827 with a starting spinning speed at 1000 rpm, with a ramping speed of 300 rm for 5 sec; and spinning at 3000 rpm, with a ramping speed of 700 rm for 40 sec.

#### *B.5.2.2 Pre-bake*

Bake the wafer on a hotplate with the temperature preset at 120°C for 1.5 min.

#### *B.5.2.3 Expose*

Use the right MJB-3 channel 1 with an intensity of 3 mW/$cm^2$ for 55 sec.

#### *B.5.2.4 Develop*

Develop with microposit 354 developer for 20 to 22 sec.

#### *B.5.2.5 Rinse*

Rinse with DI water, blow dry.

#### *B.5.2.6 Inspection*

Check features with microscope, and check the thickness with alpha-step profolometer. The thickness is about 3 $\mu$m.

#### *B.5.2.7 Bake*

Bake the wafer with a hotplate at 120°C for 50 sec.

### B.5.3 Etch $Si_3N_4$ using Plasma Therm RIE

#### *B.5.3.1 Clean Chamber*

Run clean process for 1 hour.

#### *B.5.3.2 Wafer Loading*

Move the wafer into the chamber.

#### *B.5.3.3 $Si_3N_4$ Etching*

Etch $Si_3N_4$ for 5 to 6 min, using recipe: EM_SIN.set.

#### *B.5.3.4 Inspection*

Check features with microscope to make sure the $Si_3N_4$ in the open area has been etched completely. If not, place the wafer back to the Plasma Therm RIE and continue to etch until it's completely etched.

#### *B.5.3.5 Clean*

Remove the photoresist with Acetone, blow dry.

#### *B.5.3.6 Descum*

Run oxygen plasma clean for 5 min using Plasma Therm RIE.

## *B.6 Backside Ground Plane Electro-Plating*

### B.6.1 Protect the Front Side with Shipley SC1827

#### *B.6.1.1 Spin*

Spin Shipley SC1827 on the front side of the wafer with the spinning speed of: starting at 1000 rpm, with a ramping speed of 300 rm for 5 sec; and spinning 3000 rpm, with a ramping speed of 700 rm for 30 sec.

#### *B.6.1.2 Bake*

Bake the wafer on a hotplate with the temperature preset at 120°C for 1.5 min.

### B.6.2 Etch Ti layer

#### *B.6.2.1 Dilute HF*

Dilute HF with DI water to a concentration of HF:$H_2O$ as 1:10.

#### *B.6.2.2 Etch Ti*

Use tweezer to hold the wafer and dip it into the HF solution to etch Ti, for 4 to 6 sec. Slightly agitate.

#### *B.6.2.3 Clean*

Rinse with DI water thoroughly and blow dry.

### B.6.3 Setup Gold-plating station

#### *B.6.3.1 Connect the Wires for the Plating Station*

Two Teflon boards are used: one has the metal mesh on it to connect to the cathode, and other one has a metal clip attached to the board with a small tip which is used to be in contact with the wafer, which will be connected to the anode. These two boards are placed inside the bottle with the gold solution.

#### *B.6.3.2 Setup Plating Station Parameters*

The output current of the DC source is set at 10 mA; the probe temperature is at 55°C and the stirrer spinning speed is at 200 rpm.

### B.6.4 Electro-Plate Gold

Wait for the solution temperature stable at 55°.

#### *B.6.4.1 Connect the Wafer*

Clip the wafer onto the board that connects to the anode, make sure there is a good DC contact.

#### *B.6.4.2 Electro Plate the gold*

Plate for 35 min.

#### *B.6.4.3 Clean*

Rinse with DI water, and blow dry.

### B.6.5 Remove Photoresist on the Frontside

#### *B.6.5.1 Clean*

Clean wafer with Acetone and IPA, blow dry.

#### *B.6.5.2 Bake*

Bake wafer on a hotplate at 120°C for 2 min.

## *B.7 Protect the Backside Using Shipley SC1827*

### B.7.1 Spin

Spin Shipley SC1827 on the backside of the wafer with the following spinning speed: starting at 1000 rpm, with a ramping speed of 300 rm for 5 sec; and spinning as 3000 rpm, with a ramping speed of 700 rm for 30 sec.

### B.7.2 Bake

Bake the wafer on a hotplate preset at 120°C for 1.5 min.

## *B.8 Sacrificial Layer Patterning Using Shipley SC1813 (Clear Field Mask)*

### B.8.1 Spin

Spin SC 1813 on the wafer as the following speed: starting at 700 rpm, with a ramping speed of 200 rm for 5 sec; and spinning at 2000 rpm, with a ramping speed of 500 rm for 40 sec.

### B.8.2 Bake

Bake the wafer on a hotplate at 120°C for 1.5 min.

### B.8.3 Expose

Expose with the right MJB-3 channel 1 with an intensity of 3 mW/$cm^2$ for 50 sec.

### B.8.4 Develop

Develop with microposit 354 for 20 to 22 sec.

### B.8.5 Clean

Rinse with DI water and blow dry.

### B.8.6 Inspection

Check features with microscope, and check the thickness with the alpha-step profolometer. The thickness is about 2 $\mu$m.

### B.8.7 Bake

Bake wafer on hotplate at 125°C for 1 min.

## *B.9 Membrane Layer Formation (Dark Field Mask)*

### B.9.1 Seed Layer Deposition with E-beam Evaporator

This step must be done immediately after the sacrificial layer patterning.

Use E-beam evaporator to deposit Ti/Au/Ti for a thickness of 300/2500/200 $\mathring{A}$, with the deposition rate of 2 $\mathring{A}$/sec for each material, and the vacuum at 2.0 x $10^{-6}$ or lower.

### B.9.2 Pattern with Shipley SC1827 (Very important)

#### *B.9.2.1 Spin*

Spin SC1827 with the following spinning speed: starting at 1000 rpm, with a ramping speed of 300 rm for 5 sec; and spinning at 3000 rpm, with a ramping speed of 700 rm for 40 sec.

#### *B.9.2.2 Pre-bake*

Bake the wafer at 75°C in the oven for 20 min.

#### *B.9.2.3 Expose*

Use the right MJB-3 channel 1 with an intensity of 3 mW/$cm^2$ for 55 sec.

#### *B.9.2.4 Develop*

Develop with microposit 354 developer for 20 to 22 sec.

#### *B.9.2.5 Rinse*

Rinse with DI water, blow dry.

#### *B.9.2.6 Inspection*

Check features with microscope, and check the thickness with the alpha-step profolometer. The thickness is about 3 $\mu$m.

### B.9.3 Setup Gold-plating station

#### *B.9.3.1 Connect the Wires for the Plating Station*

Two Teflon boards are used: one has the metal mesh on it to connect to the cathode, and other one has a metal clip attached to the board with a small tip which is used to be in contact with the wafer, which will be connected to the anode. These two boards are placed inside the bottle with the gold solution.

#### *B.9.3.2 Setup Plating Station Parameters*

The output current of the DC source is set at 7.8 mA; the probe temperature is at 55°C and the stirrer spinning speed is at 200 rpm.

### B.9.4 Electro-Plate Gold

Wait for the solution temperature stable at 55°.

#### *B.9.4.1 Connect the Wafer*

Clip the wafer onto the board that connects to the anode, make sure there is a good DC contact.

#### *B.9.4.2 Electro Plate the gold*

Plate for 25 min.

#### *B.9.4.3 Clean*

Rinse with DI water, and blow dry.

#### *B.9.4.4 Inspection*

Check with thickness of the plated gold, which is around 2 $\mu$m.

### B.9.5 Remove membrane Seed layer

#### *B.9.5.1 Remove photoresist*

Flood expose the right MJB-3 channel 1 for 1.5 min.

#### *B.9.5.2 Develop*

Develop with microposit 354 developer for 1 min.

#### *B.9.5.3 Clean*

Rinse with DI water and blow dry.

#### *B.9.5.4 Etch Ti*

Etch Ti with HF:$H_2$O as 1:10 for 4 to 6 sec.

#### *B.9.5.5 Clean*

Rinse with DI water thoroughly, blow dry.

#### *B.9.5.6 Etch Au*

Etch Au with gold etchant for 15 sec.

#### *B.9.5.7 Clean*

Rinse with DI water thoroughly, blow dry.

#### *B.9.5.8 Etch Ti*

Etch Ti with HF:$H_2O$ as 1:10 for 4 to 6 sec.

#### *B.9.5.9 Clean*

Rinse with DI water thoroughly, blow dry.

## *B.10 Remove Photoresist from the Backside*

### B.10.1 Flood Expose

Flood Expose with the right MJB-3 channel 1 for 1.5 min.

### B.10.2 Develop

Develop with microposit 354 developer for 1 min.

### B.10.3 Clean

Rinse with DI water, blow dry.

## *B.11 Sacrificial Layer Removal*

### B.11.1 Soak into the Photoresist Stripper

Pour photoresist stripper 1112A into a beaker and soak the wafer into the beaker.

### B.11.2 Heat Up the Solution

Cover the beak with a sheet of aluminum foil, and move it onto a hotplate with the temperature preset at 65°C. Leave it on the hotplate for about 8 hours.

## *B.12 Dry with critical point dryer*

### B.12.1 Wafer transfer to DI Water

Move the beaker off the hotplate, then carefully transfer the wafer from the photoresist stripper into a beaker with DI water, wait for few sec.

### B.12.2 Clean with DI water

Transfer the wafer into another beaker with DI water. Repeat this twice very carefully.

### B.12.3 Wafter Transfer to IPA

Transfer the wafer into a beaker with IPA, wait for few sec, then transfer it into another beaker with IPA. Repeat for twice carefully.

### B.12.4 Wafer Transfer to Critical Point Dryer

Pour IPA into the chamber of the critical point dryer, transfer the wafer from the beaker with IPA into the chamber.

### B.12.5 Dry

Run Critical point dryer.

## *B.13 Fabrication Done*

# APPENDIX C

# THE MEASURED DISCONTINUITY S-PARAMETERS FOR THE WIRE BONDS FROM THE SILICON WAFER USED FOR THE IMPEDANCE TUNERS TO THE TMM6 BOARD USED FOR THE POWER AMPLIFIERS

| Frequency (GHz) | $S_{11}$ Mag/Angle | $S_{21}$ Mag/Angle | $S_{12}$ Mag/Angle | $S_{22}$ Mag/Angle |
|---|---|---|---|---|
| 9.5 | 0.0948/169.3 | 0.9871/79.82 | 0.9871/79.82 | 0.0948/169.3 |
| 9.6 | 0.1018/167.47 | 0.9853/79.4 | 0.9853/79.4 | 0.1018/167.47 |
| 9.7 | 0.1091/165.64 | 0.9835/79.04 | 0.9835/79.04 | 0.1091/165.64 |
| 9.8 | 0.1109/163.74 | 0.9813/78.76 | 0.9813/78.76 | 0.1109/163.74 |
| 9.9 | 0.1266/162.52 | 0.9782/78.36 | 0.9782/78.36 | 0.1266/162.52 |
| 10 | 0.1361/160.92 | 0.9747/78.12 | 0.9747/78.12 | 0.1361/160.92 |
| 10.1 | 0.1467/160.26 | 0.9725/77.84 | 0.9725/77.84 | 0.1467/160.26 |
| 10.2 | 0.1599/159.45 | 0.9694/77.49 | 0.9694/77.49 | 0.1599/159.45 |
| 10.3 | 0.1735/158.96 | 0.9653/77.17 | 0.9653/77.17 | 0.1735/158.96 |
| 10.4 | 0.1899/158.43 | 0.96/76.88 | 0.96 76.88 | 0.1899/158.43 |
| 10.5 | 0.2032/157.94 | 0.9568/76.67 | 0.9568 76.67 | 0.2032/157.94 |

# APPENDIX D

# FABRICATION PROCESS RECIPE FOR RECONFIGURABLE IMPEDANCE TUNER - DC CONTACT MEMS SWITCH FABRICATION PROCESS

## *D.1 Wafer Preparation*

### D.1.1 Wafer Dicing

Use diamond pen to dice a full 4" wafer into 4 pieces.

### D.1.2 Clean

Soak the wafer in Actone and then IPA (Isopropyl Alcohol) for 5 minutes with each solvent, respectively.

### D.1.3 Dry

Blow dry the wafer with Nitrogen gun, and soft bake for 2 min on a hotplate preset temperature at 120°C.

## *D.2 $SiO_2$ Deposition*

Use STS or Unaxis PECVD to deposit 1 $\mu$m of $SiO_2$ on top of the silicon wafer.

### D.2.1 Deposit $SiO_2$ with STS PECVD

#### *D.2.1.1 Run Clean Process*

Run clean process for 2 hours, using recipe: clean.set.

#### *D.2.1.2 Run Deposition Process*

Deposit $SiO_2$ for 15 min to a thickness of 1 $\mu$m, using recipe: lfsin.set

### D.2.2 Deposit $SiO_2$ with Unaxis PECVD

#### *D.2.2.1 Run Clean Process*

Run clean process for 2 hours, using recipe: clean_250.set. This makes sure the clean process is done at 250°.

#### *D.2.2.2 Run Deposition Process*

Deposit $SiO_2$ for 25 to a thickness of 1 $\mu$m, using recipe: EM_sin.set. The deposition is done at 250°C.

## *D.3 ITO and AZO Patterning (clear field mask)*

### D.3.1 Deposition

The deposition of ITO and AZO is done at nGimat to achieve the desired sheet resistance, by using CCVD.

### D.3.2 Patterning with Shipley SC1827

#### *D.3.2.1 Spin*

Spin SC1827 with the spinning speed as: starting at 1000 rpm, with a ramping speed of 300 rm for 5 sec; spinning at 3000 rpm, with a ramping speed of 700 rm for 40 sec.

#### *D.3.2.2 Bake*

Bake the wafer on a hotplate with temperature preset at 120°C for 1.5 min.

#### *D.3.2.3 Expose*

Expose with the right MJB-3 channel 1 with the intensity of 3 mW/$cm^2$ for 55 sec.

#### *D.3.2.4 Develop*

Develop with microposit 354 developer for 20 to 22 sec.

#### *D.3.2.5 Clean*

Rinse with DI water, blow dry.

#### *D.3.2.6 Inspection*

Check features with the microscope to make sure features are fully developed, and check the thickness with the alpha-step profolometer. The thickness is about 3 $\mu$m.

### D.3.3 Etch ITO or AZO

#### *D.3.3.1 Etch ITO*

Mix the following chemicals for the concentration of 36% HCl:64% HN$O_3$: $H_2$O as 4:2:1. Etch for 15 to 20 sec.

#### *D.3.3.2 Etch AZO*

Mix the chemicals for the concentration of 36%HCl:$H_2$O as 1:10, etch for 15 to 20 sec.

#### *D.3.3.3 Clean*

Rinse with DI water thoroughly, blow dry.

#### *D.3.3.4 Inspection*

Check with microscope to make sure it's fully etched.

### D.3.4 Clean

Remove the photoresist with Acetone and IPA, blow dry.

### D.3.5 Bake

Bake the wafer on a hotplate with the temperature preset at 120°C for 5 min.

## *D.4 Bottom Electrode Lift-Off (clear field mask)*

### D.4.1 Pattern with Clariant AZ5214

#### *D.4.1.1 Spin*

Spin AZ5214 on the wafer with the following speed: start with 1000 rpm, with a ramping speed of 300 rm for 5 sec; then spin at 3000 rpm, with a ramping speed of 700 rm, for 30 sec.

#### *D.4.1.2 Pre-Bake*

Bake the wafer on a hotplate at 110°C for 1.5 min.

#### *D.4.1.3 Expose*

Expose with the right MjB-3 channel 1 with the intensity of 3 mW/$cm^2$, for 12 sec.

#### *D.4.1.4 Post-Bake*

Bake the wafer on a hotplate at 120°C for 2 min.

#### *D.4.1.5 Flood Expose*

Remove the mask from MJB-3 and flood expose the wafer for 1.5 min.

#### *D.4.1.6 Develop*

Develop with Microposit 354 Developer for 20 to 22 sec; or AZ 400k: $H_2O$ as 1:4 for 20 sec.

#### *D.4.1.7 Clean*

Rinse with DI water, blow dry.

#### *D.4.1.8 Inspect*

check features with the microscoope and the thickness with alpha-step profolometer. The thickness is about 1.2 $\mu$m.

#### *D.4.1.9 Bake*

Bake yhr wafer on s hotplate at 120°C for 50 sec.

### D.4.2 Deposit Metal with E-Beam Evaporator

#### *D.4.2.1 Wafer Mounting*

Mount the wafer on the wafer holder and place it inside the E-beam evaporator chamber.

#### *D.4.2.2 Deposition*

Deposit Ti/Au for the thickness of 300/2000 $\mathring{A}$ starting with the vacuum at 2.0x10$^{-6}$ torr. Deposition rate is 2 $\mathring{A}$/sec for both materials.

### D.4.3 Lift-off

#### *D.4.3.1 Soak with Acetone*

Soak the wafer into a beaker with Acetone. Vibrate with ultra-sonic bath for 30 sec to 1 min, take the wafer out of the beaker, and clean the beaker with the DI water. Fill the beaker with Actone and leave the wafer in the beaker for 1 to 2 hours.

#### *D.4.3.2 Rinse*

Rinse with DI water, blow dry.

#### *D.4.3.3 Inspection*

Check features to make sure the lift-off is done successfully.

#### *D.4.3.4 Bake*

Bake the wafer at 120°C for 2 min.

## *D.5 Backside E-beam Deposition*

### D.5.1 Wafer Mounting

Mount the wafer on the wafer holder and place it inside the E-beam evaporator chamber.

### D.5.2 Deposition

Deposit Ti/Au for the thickness of 300/2000 $\mathring{A}$ starting with the vacuum at 2.0x10$^{-6}$ torr. Deposition rate is 2 $\mathring{A}$/sec for both materials.

## *D.6 $Si_3N_4$ Patterning (Dark Field Mask)*

### D.6.1 $Si_3N_4$ Deposition with Unaxis PECVD

#### *D.6.1.1 Chamber Clean*

Run clean process at 250°C, using recipe clean_250.set.

#### *D.6.1.2 Wafer Loading*

Move wafer into the chamber.

#### *D.6.1.3 $Si_3N_4$ Deposition*

Deposit $Si_3N_4$ for 35 min to a thickness of 3000 $\mathring{A}$, using recipe EM_SIN_250.set.

### D.6.2 Pattern with Shipley SC1827

#### *D.6.2.1 Spin*

Spin SC1827 with a starting spinning speed at 1000 rpm, with a ramping speed of 300 rm for 5 sec; and spinning at 3000 rpm, with a ramping speed of 700 rm for 40 sec.

#### *D.6.2.2 Pre-bake*

Bake the wafer on a hotplate with the temperature preset at 120°C for 1.5 min.

#### *D.6.2.3 Expose*

Use the right MJB-3 channel 1 with an intensity of 3 mW/$cm^2$ for 55 sec.

#### *D.6.2.4 Develop*

Develop with microposit 354 developer for 20 to 22 sec.

#### *D.6.2.5 Rinse*

Rinse with DI water, blow dry.

#### *D.6.2.6 Inspection*

Check features with microscope, and check the thickness with alpha-step profolometer. The thickness is about 3 $\mu$m.

#### *D.6.2.7 Bake*

Bake the wafer with a hotplate at 120°C for 50 sec.

### D.6.3 Etch $Si_3N_4$ using Plasma Therm RIE

#### *D.6.3.1 Clean Chamber*

Run clean process for 1 hour.

#### *D.6.3.2 Wafer Loading*

Move the wafer into the chamber.

#### *D.6.3.3 $Si_3N_4$ Etching*

Etch $Si_3N_4$ for 5 to 6 min, using recipe: EM_SIN.set.

#### *D.6.3.4 Inspection*

Check features with microscope to make sure the $Si_3N_4$ in the open area has been etched completely. If not, place the wafer back to the Plasma Therm RIE and continue to etch until it's completely etched.

#### *D.6.3.5 Clean*

Remove the photoresist with Acetone, blow dry.

#### *D.6.3.6 Descum*

Run oxygen plasma clean for 5 min using Plasma Therm RIE.

## *D.7 Seed Layer Deposition*

### D.7.1 Front Side Deposition

Use E-beam evaporator to deposit Ti/Au/Ti for a thickness of 300/2500/200 $\mathring{A}$, with the deposition rate of 2 $\mathring{A}$/sec for each material, and the vacuum at 2.0 x $10^{-6}$ torr or lower.

### D.7.2 Back Side Deposition

Use E-beam evaporator to deposit on the backside: Ti/Au/Ti for a thickness of 300/3000/200 $\mathring{A}$, with the rate of 3 $\mathring{A}$/sec.

## *D.8 Backside Ground Plane Electro-Plating*

### D.8.1 Protect the Front Side with Shipley SC1827

#### *D.8.1.1 Spin*

Spin Shipley SC1827 on the front side of the wafer with the spinning speed of: starting at 1000 rpm, with a ramping speed of 300 rm for 5 sec; and spinning 3000 rpm, with a ramping speed of 700 rm for 30 sec.

#### *D.8.1.2 Bake*

Bake the wafer on a hotplate with the temperature preset at 120°C for 1.5 min.

### D.8.2 Etch Ti layer

#### *D.8.2.1 Dilute HF*

Dilute HF with DI water to a concentration of HF:$H_2O$ as 1:10.

#### *D.8.2.2 Etch Ti*

Use tweezer to hold the wafer and dip it into the HF solution to etch Ti, for 4 to 6 sec. Slightly agitate.

#### *D.8.2.3 Clean*

Rinse with DI water thoroughly and blow dry.

### D.8.3 Setup Gold-plating station

#### *D.8.3.1 Connect the Wires for the Plating Station*

Two Teflon boards are used: one has the metal mesh on it to connect to the cathode, and other one has a metal clip attached to the board with a small tip which is used to be in contact with the wafer, which will be connected to the anode. These two boards are placed inside the bottle with the gold solution.

#### *D.8.3.2 Setup Plating Station Parameters*

The output current of the DC source is set at 10 mA; the probe temperature is at 55°C and the stirrer spinning speed is at 200 rpm.

### D.8.4 Electro-Plate Gold

Wait for the solution temperature stable at 55°.

#### *D.8.4.1 Connect the Wafer*

Clip the wafer onto the board that connects to the anode, make sure there is a good DC contact.

#### *D.8.4.2 Electro Plate the gold*

Plate for 35 min.

#### *D.8.4.3 Clean*

Rinse with DI water, and blow dry.

### D.8.5 Remove Photoresist on the Frontside

#### *D.8.5.1 Clean*

Clean wafer with Acetone and IPA, blow dry.

#### *D.8.5.2 Bake*

Bake wafer on a hotplate at 120°C for 2 min.

## *D.9 Protect the Backside Using Shipley SC1827*

### D.9.1 Spin

Spin Shipley SC1827 on the backside of the wafer with the following spinning speed: starting at 1000 rpm, with a ramping speed of 300 rm for 5 sec; and spinning as 3000 rpm, with a ramping speed of 700 rm for 30 sec.

### D.9.2 Bake

Bake the wafer on a hotplate preset at 120°C for 1.5 min.

## *D.10 Bottom Contact Metal Pattern (dark field mask)*

### D.10.1 Pattern the Front Side with Shipley SC1827

#### *D.10.1.1 Spin Photoresist*

Spin SC1827 starting at 1000 rpm, with a ramping speed of 300 rm for 5 sec; and spinning at 3000 rpm, with a ramping speed of 700 rm for 40 sec.

#### *D.10.1.2 Pre-bake*

Bake the wafer on a hotplate with the temperature preset at 120°C for 1.5 min.

#### *D.10.1.3 Exposure*

Expose with the right MJB-3 channel 1 with the intensity of 3 mW/$cm^2$ for 55 sec.

#### *D.10.1.4 Develop*

Develop with microposit 354 developer for 20 to 22 sec.

#### *D.10.1.5 Clean*

Rinse with DI water, blow dry.

#### *D.10.1.6 Inspection*

Check features with microscope and the thickness with alpha-step profolometer. The thickness is about 3.0 $\mu$m.

### D.10.2 Setup Gold-plating station

#### *D.10.2.1 Connect the Wires for the Plating Station*

Use the same setup as above.

#### *D.10.2.2 Setup Plating Station Parameters*

The output current of the DC source is set at 7.8 mA; the probe temperature is at 55°C and the stirrer spinning speed is at 200 rpm.

### D.10.3 Electro Plate Gold

#### *D.10.3.1 Connect the Wafer*

Clip the wafer onto the board that connects to the anode, make sure there is a good DC connection.

#### *D.10.3.2 Electro Plate the gold*

Plate for 30 min.

#### *D.10.3.3 clean*

Rinse with DI water, blow dry.

#### *D.10.3.4 Inspection*

Check features with microscope; then check thickness with alpha-step profolometer, make sure the plated gold is about 3 $\mu$m thick. If not, the wafer needs to be placed back to the plating station and continue with the gold plating. This step repeats until the plated thickness is about 3 $\mu$m.

### D.10.4 Remove Seed layer

#### *D.10.4.1 Remove photoresist*

Flood expose the front side of the wafer with right MJB-3 channel 1 for 1.5 min.

#### *D.10.4.2 Develop*

Develop with microposit 354 developer for 1 min.

#### *D.10.4.3 Rinse*

Rinse with DI water and blow dry.

#### *D.10.4.4 Etch Ti*

Etch Ti with HF:$H_2$O as 1:10 for 4 to 6 sec.

#### *D.10.4.5 Rinse*

Rinse with DI water thoroughly, blow dry.

#### *D.10.4.6 Etch Au*

Etch Au with gold etchant for 15 sec.

#### *D.10.4.7 Rinse*

Rinse with DI water thoroughly, blow dry.

#### *D.10.4.8 Etch Ti*

Etch Ti with HF:$H_2$O as 1:10 for 4 to 6 sec.

#### *D.10.4.9 Rinse*

Rinse with DI water thoroughly, blow dry.

#### *D.10.4.10 Clean*

Clean the wafer with Actone and IPA, to remove the photoresist on the backside of the wafer.

#### *D.10.4.11 Bake*

Bake the wafer on hotplate at 120°C for 2 min.

## *D.11 Protect the Backside Using Shipley SC1827*

### D.11.1 Spin

Spin Shipley SC1827 on the backside of the wafer with the following spinning speed: starting at 1000 rpm, with a ramping speed of 300 rm for 5 sec; and spinning as 3000 rpm, with a ramping speed of 700 rm for 30 sec.

### D.11.2 Bake

Bake the wafer on a hotplate preset at 120°C for 1.5 min.

## *D.12 Sacrificial Layer Patterning Using Shipley SC1813 (clear field mask)*

### D.12.1 Spin

Spin SC1813 on the wafer: starts at ramping at 700 rpm, with a ramping speed of 200 rm for 5 sec; then spin at 2000 rpm, with a ramping speed of 500 rm for 40 sec.

### D.12.2 Bake

Bake the wafer on a hotplate at 120°C for 1.5 min.

### D.12.3 $1^{st}$ Expose

Expose with the right MJB-3 channel 1 with the intensity of 3 mW/$cm^2$ for 7 sec with mask 1 to create the dimple.

### D.12.4 $2^{nd}$ Expose

Expose with the right MJB-3 channel 1 with the intensity of 3 mW/$cm^2$ for 40 sec with mask 2 to create the sacrificial layer.

### D.12.5 Develop

Develop with microposit 354 for 20 to 22 sec.

### D.12.6 Clean

Rinse with DI water and blow dry.

### D.12.7 Inspection

Check features under the microscope, and the thickness with the alpha-step profolometer. The thickness is about 2 $\mu$m.

### D.12.8 Bake

Bake the wafer on hotplate at 125°C for 1 min.

## *D.13 Membrane Seed Layer Deposition with E-beam Evaporator*

This step must be done immediately after the sacrificial layer patterning.

### D.13.1 Seed Layer Deposition

Use E-beam evaporator to deposit Ti/Au/Ti for a thickness of 300/2500/200 $\mathring{A}$, with the deposition rate of 2 $\mathring{A}$/sec for each material, and the vacuum at 2.0 x $10^{-6}$ or lower.

### D.13.2 Inspection

Check sacrificial layer under the microscope to make sure they are good. No bubbles should be observed.

## *D.14 Membrane layer formation (dark field mask)*

### D.14.1 Pattern with Shipley SC1827 (Very important)

#### *D.14.1.1 Spin*

Spin SC1827 with the speed of: starting at 1000 rpm, with a ramping speed of 300 rm for 5 sec; and spinning at 3000 rpm, with a ramping speed of 700 rm for 40 sec.

#### *D.14.1.2 Pre-bake*

Bake the wafer at 75°C in the oven for 20 min.

#### *D.14.1.3 Expose*

Expose with the right MJB-3 channel 1 with the intensity of 3 mW/$cm^2$ for 55 sec.

#### *D.14.1.4 Develop*

Develop with microposit 354 developer for 20 to 22 sec.

#### *D.14.1.5 Clean*

Rinse with DI water, blow dry.

### D.14.2 Inspection

Check features under the microscope, and thickness with the alpha-step profolometer. The thickness is about 3 $\mu$m.

### D.14.3 Setup Gold-plating station

#### *D.14.3.1 Connect the Wires for the Plating Station*

Two Teflon boards are used: one has the metal mesh on it to connect to the cathode, and other one has a metal clip attached to the board with a small tip which is used to be in contact with the wafer, which will be connected to the anode. These two boards are placed inside the bottle with the gold solution.

#### *D.14.3.2 Setup Plating Station Parameters*

The output current of the DC source is set at 7.8 mA; the probe temperature is at 55°C and the stirrer spinning speed is at 200 rpm.

### D.14.4 Electro-Plate Gold

Wait for the solution temperature stable at 55°.

#### *D.14.4.1 Connect the Wafer*

Clip the wafer onto the board that connects to the anode, make sure there is a good DC contact.

#### *D.14.4.2 Electro Plate the gold*

Plate for 25 min.

#### *D.14.4.3 Clean*

Rinse with DI water, and blow dry.

#### *D.14.4.4 Inspection*

Check with thickness of the plated gold, which is around 2 $\mu$m.

### D.14.5 Remove membrane Seed layer

#### *D.14.5.1 Remove photoresist*

Flood expose the right MJB-3 channel 1 for 1.5 min.

#### *D.14.5.2 Develop*

Develop with microposit 354 developer for 1 min.

#### *D.14.5.3 Clean*

Rinse with DI water and blow dry.

#### *D.14.5.4 Etch Ti*

Etch Ti with HF:$H_2$O as 1:10 for 4 to 6 sec.

#### *D.14.5.5 Clean*

Rinse with DI water thoroughly, blow dry.

#### *D.14.5.6 Etch Au*

Etch Au with gold etchant for 15 sec.

#### *D.14.5.7 Clean*

Rinse with DI water thoroughly, blow dry.

#### *D.14.5.8 Etch Ti*

Etch Ti with HF:$H_2$O as 1:10 for 4 to 6 sec.

#### *D.14.5.9 Clean*

Rinse with DI water thoroughly, blow dry.

## *D.15 Remove Photoresist from the Backside*

### D.15.1 Flood Expose

Flood Expose with the right MJB-3 channel 1 for 1.5 min.

### D.15.2 Develop

Develop with microposit 354 developer for 1 min.

### D.15.3 Clean

Rinse with DI water, blow dry.

## *D.16 Sacrificial Layer Removal*

### D.16.1 Soak into the Photoresist Stripper

Pour photoresist stripper 1112A into a beaker and soak the wafer into the beaker.

### D.16.2 Heat Up the Solution

Cover the beak with a sheet of aluminum foil, and move it onto a hotplate with the temperature preset at 65°C. Leave it on the hotplate for about 8 hours.

## *D.17 Dry with critical point dryer*

### D.17.1 Wafer transfer to DI Water

Move the beaker off the hotplate, then carefully transfer the wafer from the photoresist stripper into a beaker with DI water, wait for few sec.

### D.17.2 Clean with DI water

Transfer the wafer into another beaker with DI water. Repeat this twice very carefully.

### D.17.3 Wafter Transfer to IPA

Transfer the wafer into a beaker with IPA, wait for few sec, then transfer it into another beaker with IPA. Repeat for twice carefully.

### D.17.4 Wafer Transfer to Critical Point Dryer

Pour IPA into the chamber of the critical point dryer, transfer the wafer from the beaker with IPA into the chamber.

### D.17.5 Dry

Run Critical point dryer.

## *D.18 Fabrication Done*

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